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Fabrication of low-noise carbon nanotube field-effect transistor biosensors

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***Abstract* — We report the fabrication of suspended carbon nanotube field effect transistors (CNT FETs) designed for biological sensing applications. We compare the electrical properties of our suspended CNT FET design to standard surface based CNT FETs. In particular, we show a reduction in environmental noise, suggesting that the new sensor design is a promising candidate for low-noise sensing applications.**

I. Introduction

The two-terminal resistance of a semiconducting carbon nanotube (CNT) device is sensitive to the binding of biomolecules onto the CNT surface. Several groups have demonstrated this effect using CNTs lying on substrates [1], however, there are compelling reasons to perform biosensor experiments using suspended CNT devices. Suspended CNTs are a significant distance away from charge traps in the dielectric substrate. These charge traps introduce environmental noise and limit the sensitivity of CNT-based electronic sensors [2-4]. Suspended CNT devices also allow measurements of the interactions between biomolecules and CNTs without interference from the substrate.

Here we describe the development of suspended carbon nanotube field effect transistors (CNT FETs) that are specifically designed for biological sensing applications. Our fabrication process produces suspended CNT with clean surfaces and minimal environmental noise. The electrode layout is compatible with a microfluidic system for delivering biological molecules to the sensor.

II. Biosensor Fabrication

Our suspended CNT FET biosensors satisfy the following design constraints:

(i) Transistor channels consist of a single semiconducting CNT that does not touch the underlying dielectric substrate.
(ii) The CNT surface is free of contaminates such as photoresist residue.
(iii) The electrode geometry is compatible with fluid delivery.
(iv) The fabrication process is time/cost effective.

The key fabrication steps are based on previous work by Kong et al.[5] and Cao et al. [6]. These steps are illustrated in Figure 1. An important modification to previous recipes is the introduction of a reactive ion etch (Fig. 1c) which streamlines the process.

Our starting substrate is a 6 inch $Si_3N_4/SiO_2/Si$ wafer. The top layer consists of CVD grown Si_3N_4 (100 nm thickness) on top of thermally grown SiO_2 (1 μm thickness). For future devices we plan to omit the Si_3N_4 layer because it is not necessary.

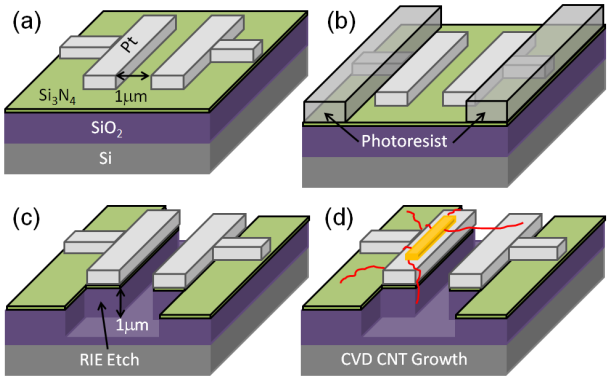

Fig. 1: Fabrication process to produce ultra-clean suspended CNTs. (a) Metal electrodes were formed by depositing a 1nm Ti sticking layer followed by 100nm Pt, forming a 1μm electrode gap. (b-c) A 20 μm wide photoresist window was patterned to serve as a mask for a 1 μm deep reactive ion etch. (d) Alumina supported catalyst was patterned on the Pt followed by a CVD fast heat growth, producing an ultra-clean suspended CNT device.

Platinum electrodes are patterned using standard photolithography and metal deposition techniques (Shipley 1813, image reversal, electron beam evaporation of a Ti sticking layer of 1 nm thickness, and a Pt layer of 100 nm thickness). The gap between the electrodes is 1 μm. It has been previously established that suspended CNTs can withstand the forces associated with liquid wetting if the suspended length is 3 μm or less.[7] The Pt electrodes extend a distance of approximately 1 cm away from the gap. The long electrode length makes it possible to clamp microfluidic channels onto the device while still performing electrical characterization.

A second patterning step is used to etch the SiO_2 substrate. A 20 μm window is created in a photoresist layer

(Shipley 1813) and reactive ion etching (RIE) is used to remove the 100 nm Si_3N_4 layer and 900 nm of SiO_2 (Fig. 2b-c). The dielectric is masked by both the photoresist and the Pt electrodes, creating an etch pattern that is self-aligned to the electrodes. The RIE is an anisotropic process that produces a trench with vertical side walls.

A third patterning step is used to place CNT catalyst on the Pt electrodes (Fig 1d). Windows with dimension 4 μm x 14 μm are patterned in the photoresist layer. The windows are positioned on the Pt electrode and are set back 2 μm from the edge. After patterning the photoresist, the wafer is diced into 30 individual pieces and stored until the final processing step.

The final processing step is CNT growth. Directly before CNT growth, a catalyst is deposited on the chip (3.3 mM Iron(iii) nitrate nonahydrate, 1 mM Molybdenum(vi) dioxide bis(acetyl-acetonate), 9.8 mM Alumina prepared in DI H_2O solution). The liquid suspension catalyst is drop cast onto the surface, allowed to sit for 5 minutes and followed promptly by a N_2 blow dry. The chip was then rinsed with a DI H_2O squirt and followed by photoresist removal by a sequential rinse with acetone, IPA, DI H_2O and followed by an N_2 blow dry.

Fast-heat chemical vapor deposition (CVD) growth was utilized to produce pristine CNTs on top of the Pt electrodes [5]. The fast-heat method minimizes the time that Pt electrodes are exposed to high temperature conditions. Figure 2 shows scanning electron micrographs of the Pt surface after being exposed to different high temperature conditions either with or without the fast-heat method. Figure 2a shows a severely damaged Pt surface after a standard CVD growth. Temperature was ramped to T_{growth} = 850 C° in H_2 (0.45 SLM), followed by a 5 minute growth (0.45 SLM H_2 and 1.8 SLM CH_4), and cooling in Ar (1 SLM); during all steps the chip remained in the active heat zone of the furnace. Clearly, this standard CVD growth method does not preserve the integrity of the Pt electrodes. Moreover, the alumina supported catalyst becomes encapsulated in Pt and no CNT growth is observed.

The fast heat method reduces the time that the chip is exposed to the hot zone of the growth furnace. A quartz shuttle inside the one inch growth tube is used to rapidly load the substrate in and out of the hot zone. A steel washer on the cool end of the shuttle allows the operator to move the shuttle by sliding a small permanent magnet along the outside of the quartz tube. With the chip outside the hot zone, the furnace is ramped up to T_{growth}, then the chip is slid inside the hot zone for 5 minutes. Figure 2b shows the Pt surface after a fast heat growth at T_{growth} = 850°C. There is a clear improvement compared to standard growth, however, to fully preserve the integrity of the Pt we found that fast heating at T_{growth} = 820°C is preferable (Fig. 2c). This growth temperature is still high enough to produce a good yield of CNT devices [7].

For higher density growth of CNTs, it is possible to deposit more catalyst on the Pt electrode. To increase the amount of catalyst, we drop cast the liquid suspension catalyst on the chip and then evaporate all water by placing the chip on a 90°C hotplate. The resulting "mountain" of catalyst is seen in Fig. 2d. We also find that substituting CH_4-based growth with an alcohol vapor growth increases growth density. The growth conditions in Fig. 2d are T_{growth} = 820°C, 0.45 SLM H_2, 0.3 SLM Ar bubbled in ice cold ethanol and 0.15 SLM Ar bubbled in ice cold methanol. Several CNTs are visible in the top of Fig. 2d.

When using optimized CNT growth parameters we obtain 1 or 2 devices per chip that show electrical characteristics that are consistent with an individual semiconducting CNT bridging the gap between electrodes.

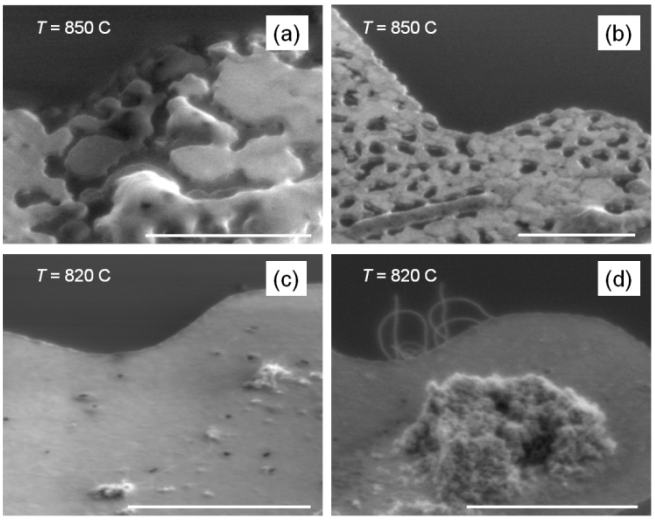

Fig. 2: SEM scans (5 μm scale bars) showing the Pt electrodes after various CVD growth time and durations. (a) Ramp up and cool in the active heat zone of furnace at 850C, CH_4 growth. (b) Fast heat CH_4 growth at 850C for 5 minutes (c) Fast heat growth CH_4 820C for 5 minutes (d) Fast heat alcohol growth with increased catalyst density, 820C for 5 minutes.

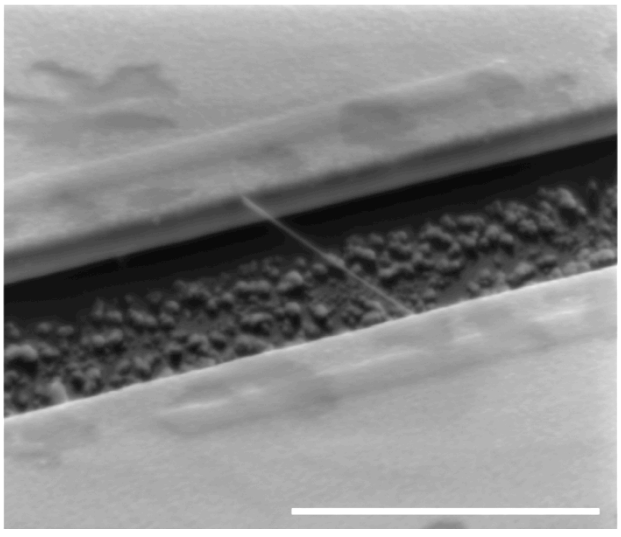

Fig. 3: SEM image (3 μm scale bar) of a single CNT bridging a gap between two gold electrodes. The CNT was placed over the trench by means of a PMMA assisted transfer, using a technique described by Jiao et al. [10]. Due to time constraints the authors were unable to attain an SEM scan of the current devices under investigation.

III. Electronic Properties of a Suspended CNT

Suspending a CNT above a dielectric surface (rather than touching the dielectric surface) can dramatically reduce the environmental noise associated with charge fluctuations at dielectric surfaces [2, 8, 9]. An SEM image of a suspended CNT device is shown in Fig. 3 illustrating the structure of our suspended CNT sensors. The CNT is well above the underlying oxide as it hangs between the two metal electrodes.

Figure 5a shows transistor characteristics of a suspended semiconducting CNT device that was produced following the fabrication process described in Section II. The characteristics were obtained in ambient conditions (room temperature, exposed to air) with a source-drain bias V_{sd} = 25 mV. For comparison, Fig. 4b shows a typical transistor characteristic of a non-suspended CNT device. As observed by previous authors, the suspended CNT device has substantially less hysteresis [2, 8, 9].

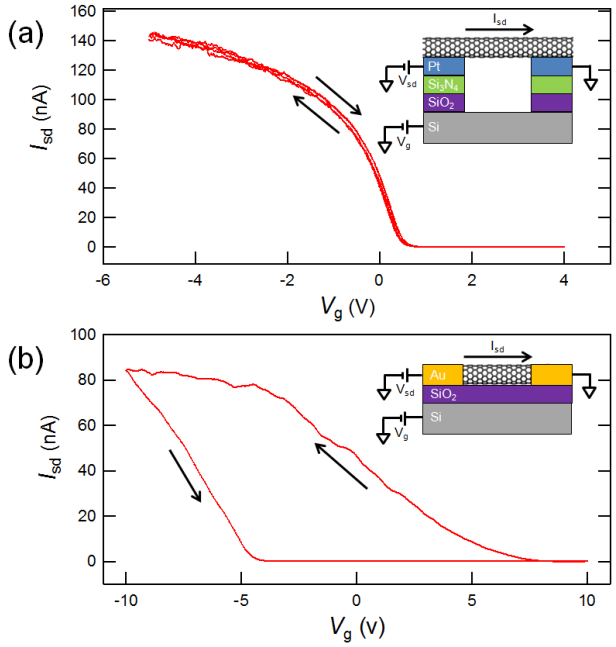

Fig. 4: Source-Drain current as a function of gate voltage (sweep rate dV_g/dt = 1 V/sec). (a) Suspended CNT grown on Pt shows very little hysteresis. (b) Surface based CNT exhibits a comparatively larger hysteresis offset.

To quantify the capacitive coupling between the global backgate and the suspended CNT, C_g/C_{total}, we have measured $I(V_g)$ in the subthreshold regime where current drops exponentially over several decades (Fig. 5a) [11]. The subthreshold slope is 300 mV/dec, differing by a factor 5 from the room temperature limit of 60 mV/dec. The subthreshold slope suggests a capacitive coupling C_g/C_{total} = 0.2.

The goal of our work is to produce sensitive transistor devices with very low levels of background noise. To investigate noise levels in a suspended CNT FET we have measured current fluctuations over a range of different gate voltages. Figure 5b shows the power spectral density of current fluctuations, $S_I(f)$, at five different values of V_g. Similar power spectral densities ($S_I \sim 1/f$) have been previously reported for CNT devices [12].

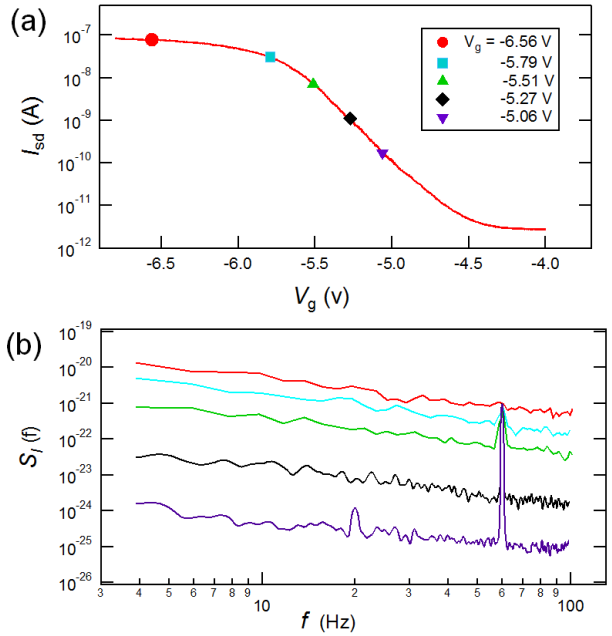

Fig. 5: (a) Semi-log plot of source-drain current as a function of gate voltage (gate sweep 10mV/sec). (b) Visualization of the Power Spectral Density for 5 different gating values, clearly showing $1/f$ dependence.

We analyze the current fluctuations using the charge noise model that was first introduced by Tersoff [13] and later experimentally verified by Mannik et al. [12]. The charge noise model assumes that fluctuations in current are caused by fluctuations in the electrostatic environment such that

$$S_I(f) = S_{input}(f)\left(\frac{dI}{dV_g}\right)^2, \qquad (1)$$

where $S_{input}(f)$ has units of V^2/Hz. Equation (1) is equivalent to the statement that $\delta I = (dI/dV_g)\delta V_g$ where δI is a fluctuation in current caused by a fluctuation in effective gate voltage δV_g.

We fit Eq. 1 to our measured data using one free parameter. Figure 6 shows measured values of S_I at f = 10 Hz compared to the line $S_{input}(10\text{ Hz})\cdot(dI/dV_g)^2$. The best fit value of $S_{input}(10\text{ Hz})$ is 0.005 mV^2/Hz. This is equivalent to an rms environmental noise of 0.75 mV when measured over a bandwidth of 0.1 – 100 Hz.

Previous experimental measurements of charge noise by Mannik et al. yielded S_{input} = 0.05 mV^2/Hz at 10 Hz for surface-bound CNT devices with a channel length of 1 μm. This previous report of S_{input} is 10 times larger than our current measurement.

The measurements of Mannik et al. were performed in electrolyte solution, therefore, it is possible that the electrolyte solution dominates environmental noise rather than charge noise in the dielectric substrate. To test this possibility, we are currently measuring our suspended CNT devices in electrolyte solutions.

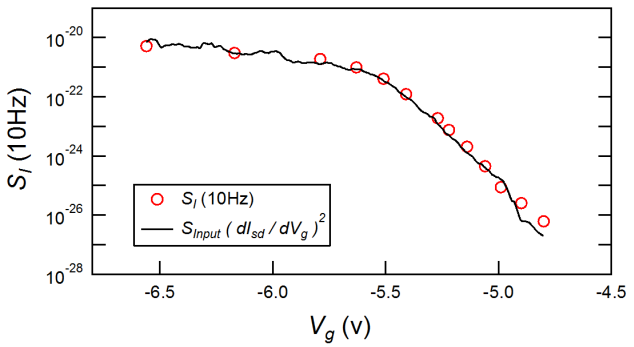

Fig. 6: Measured power spectral density S_I(10Hz) shown as red dots. The black line is the square of the numerical derivative of the source-drain current with respect to V_g multiplied by the fitting parameter S_{input}(10 Hz).

IV. Summary and Conclusion

We have fabricated suspended carbon nanotube field effect transistors that have electrode geometries suitable for integration in biological environments. We observe evidence that electrostatic fluctuations in the environment of the suspended CNT are minimized. We determine an rms electrostatic noise (stochastic modulation of the effective gate voltage) of 0.75 mV when measured over a bandwidth of 0.1 – 100 Hz. This environmental noise is significantly less than the electrostatic signals that are expected from charged proteins [14]. Therefore, suspended CNTs are a promising platform for high sensitivity biosensing applications.

Acknowledgment

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