Controlling the function of carbon nanotube devices with re-writable charge patterns

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We use atomic force microscopy lithography to write charge patterns in close proximity to carbon nanotube field-effect transistor devices. The silicon dioxide substrate retains the charge for days, allowing various charge configurations to be tested. We show that the written charge can move the Fermi level in the nanotube by 1 eV and we use this charge lithography to reconfigure a field-effect transistor into a pn junction. The substrate charge can be erased and rewritten, offering a new tool for prototyping nanodevices and optimizing electrostatic doping profiles. © *2011 American Institute of Physics*. [doi:10.1063/1.3622138]

The performance of nanoelectronic devices is highly dependent on charges in the surrounding environment. Surface charge traps give rise to device noise[1] and hysteresis,[2,3] while spatial variations in surface charge lead to gate-sensitive "hotspots" in nanoscale electronic devices[4] and light-sensitive "hotspots" in nanoscale optoelectronic devices.[5]

Previous authors have demonstrated that scanning probe lithography can be used to create charge patterns on a range of surfaces.[6–9] Such charge patterns have been used in nanoelectronics research, for example, to electrostatically define channels in a two-dimensional electron gas[6] or to create small electrostatic perturbations in carbon nanotube based field-effect transistor (CNT FET) devices.[10] In the work of Brunel *et al.*,[10] a conducting atomic force microscopy (AFM) tip was used to write a spot of charge on the SiO_2 surface near a CNT FET. The charge-sensitive CNT device detected this small electrostatic perturbation and functioned as a non-volatile memory element.

Here, we show that charge patterns written on a SiO_2 surface can be used to controllably modulate the doping profile of a nanoelectronic device. We demonstrate electrostatic doping that corresponds to ± 1 eV shifts in the Fermi level of a CNT. To illustrate the power of this charge patterning technique, we define regions of positive and negative charges in close proximity to a CNT FET and create a pn junction device.

Individual CNT devices were made by patterning catalyst on a SiO_2/Si substrate (thermal oxide with thickness $t = 300$ nm) and growing CNTs by catalyzed chemical vapor deposition using a semi-automated growth system (Kevek Innovations).[11] Electrodes (Ti/Pt) were patterned by photolithography to produce circuits with ~10 nanotubes connected in parallel. Scanning probe experiments were performed in an AFM with a custom-built stage for *in-situ* electrical probing (Asylum Research MFP-3D). Electric force microscopy (EFM)[12] and scanning gate microscopy (SGM)[4] were used to identify a single desired CNT. The undesired CNTs were electrically cut with a Pt-coated AFM probe[13] resulting in a single CNT FET. A schematic of the geometry is shown in Fig. 1.

Charge patterns were written directly on the SiO_2 layer around the CNT FET with a biased, Pt-coated AFM probe, as illustrated in Fig. 1. We found that positive and negative tip bias, V_{write}, modified the surface charge when the probe was dragged across the surface (contact force ~6–9 nN). We used a variety of scanning probe techniques to investigate this surface charge and the effect it has on the nearby CNT FET.

Fig. 2(a) shows an electrically contacted CNT on a SiO_2 substrate. Arrows on the image show the path that was traced by the electrically biased AFM tip. A tip bias $V_{write} = -10$ V was used for the upper half of the CNT, and $V_{write} = +10$ V was used in the lower half. The back gate, source, and drain electrodes were grounded during charge writing. The regions where charge was written show up clearly in Kelvin force microscopy[14] (KFM) measurements, as shown in Fig. 2(b). The KFM image confirms that negative charge was written at -10 V (the surface potential is more negative than the surrounding oxide) and positive charge was written at $+10$ V (the surface potential is more positive than the surrounding oxide).

The deposited surface charge has a dramatic effect on the doping profile of the nearby CNT. Fig. 3 shows SGM measurements taken before and after charge lithography. The SGM images are obtained by hovering the electrically

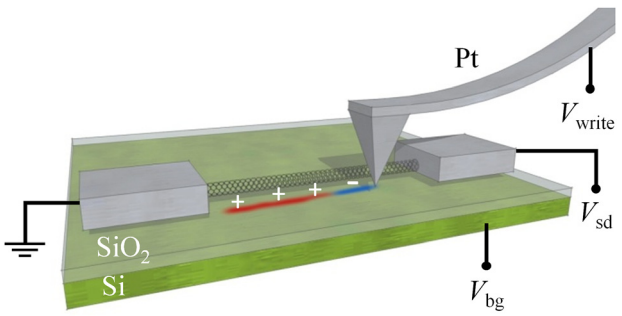

FIG. 1. (Color online) Device schematic illustrating charge lithography near a CNT connected to two electrodes (not to scale). Charge is written ~300 nm from the CNT.

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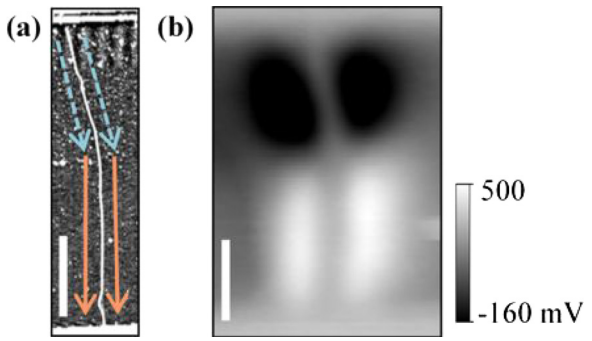

FIG. 2. (Color online) Defining the charge pattern for a pn junction. (a) AFM topography of the CNT device with arrows indicating the lithography paths (dashed line indicates $V_{write} = -10$ V, solid line indicates $V_{write} = +10$ V). (b) Kelvin force microscopy image taken after the charge lithography ($V_{bg} = 0$ V, *height* = 25 nm). Scale bars are 1 μm.

biased AFM tip (the scanning gate) above the device and recording conductance as a function of tip position.[4] The image obtained before charge lithography shows a spatially uniform response to the scanning gate, with conductance increasing when the tip is close to the CNT. After charge lithography, the SGM image shows that the upper and lower portions of the CNT respond differently to the scanning gate. Transistor curves taken before and after writing the charge also show a clear change (Fig. 3(c)). Initially, the device displayed typical small bandgap behavior with a single conductance minima at $V_{bg} = 4.3$ V. After charge lithography, the transistor curve has a double dip, with conductance minima on either side of $V_{bg} = 4.3$ V. Repeatedly sweeping V_{bg} from -1 to $+10$ V caused the two dips to approach each other and reform the original transistor curve.

The SGM measurements indicate that doping along the length of the CNT is modified by the lithographically defined surface charge. The upper portion of the CNT becomes more conductive when the negatively biased tip approaches, indicating that the upper portion of the CNT is p doped. The lower portion of the CNT becomes less conductive when the negatively biased tip approaches, indicating that the lower portion of the CNT is n doped. The transistor curves (Fig. 3(c)) further verifies that the device consists of p-type and n-type sections in series when $V_{bg} = 4.3$ V. Similar double-dip transistor curves have been observed from CNT devices that had spatially modulated doping profiles created by different means.[15]

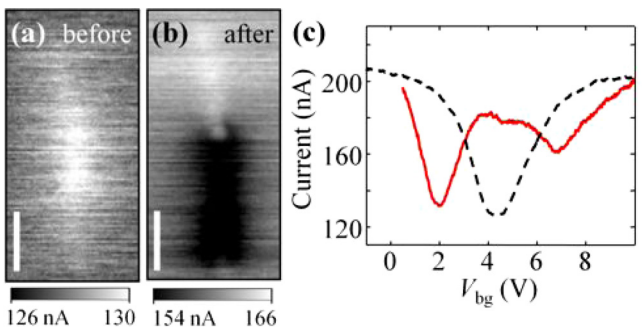

FIG. 3. (Color online) Device characteristics following pn junction engineering. (a) Scanning gate microscopy image before charge writing ($V_{bg} = 2$ V, $V_{tip} = 0$ V, $V_{sd} = 25$ mV, *height* = 25 nm). (b) Scanning gate microscopy image after charge writing ($V_{bg} = 2.5$ V, $V_{tip} = -2$ V, $V_{sd} = 25$ mV, *height* = 25 nm). Scale bars are 1 μm in both images. (c) $I(V_{bg})$ of the device shown in (a) measured with $V_{sd} = 25$ mV. The dashed black line was measured before charge writing, the solid red line was measured after charge writing.

To quantify the electrostatic doping seen in Fig. 3, we created a uniform doping profile along a CNT FET. The procedure was the same as outlined in Fig. 2(a), except that $V_{write} = +10$ V was used throughout the process. Transistor curves measured before and after showed a maximum shift $\Delta V_{bg} = -5$ V (Fig. 4(a)). Subsequent sweeps of V_{bg} (numbered 1 to 12 in Fig. 4) caused the doping effect to decay.

From the observed shift, ΔV_{bg}, one can estimate the change in Fermi level in the CNT, ΔE_F, and the linear charge density, λ_{litho}, stored on the SiO_2 surface. First, we note that the patterned charge is acting as a "side gate" and is equivalent to applying +5 V to the back gate. The charge per unit length that is induced in the CNT is then $\Delta\lambda_{CNT} = C'_{bg}\,\Delta V_{bg}$, where C'_{bg} is the back gate capacitance per unit length,[16]

$$C'_{bg} = \frac{2\pi\varepsilon\varepsilon_0}{\cosh^{-1}(t/r)} = 40\frac{\text{aF}}{\mu\text{m}}. \quad (1)$$

For our device, the radius of the CNT is $r = 1.9$ nm, the relative dielectric constant of the SiO_2 is $\varepsilon = 4$, and the thickness of the dielectric $t = 300$ nm. We find $\Delta\lambda_{CNT} = 1200e\ \mu\text{m}^{-1}$. This doping level can be expressed as a shift in the Fermi level of the CNT, $\Delta E_F = \Delta\lambda_{CNT}/eD$, where $D \approx 4/hv_F$ is the density of states of a single-walled CNT at energies above and below the bandgap (e is the charge of the electron, h is Plank's constant, and $v_F = 8 \times 10^5$ m/s is the Fermi velocity). For our experiment, we find $\Delta E_F \sim 1$ eV. If larger doping levels were required, one could pattern additional lines of charge or decrease the separation distance between λ_{litho} and the CNT. However, $\Delta E_F = \pm 1$ eV is sufficient for most semiconductor devices that utilize doping modulation.

The magnitude of the patterned charge, λ_{litho}, is proportional to $\Delta\lambda_{CNT}$. The proportionality constant depends on the ratio of capacitances C'_{tot}/C'_{sg}, where C'_{tot} is the total capacitance between the patterned charge and nearby conducting objects and C'_{sg} is the "side gate" capacitance between the patterned charge and the CNT (Fig. 4(b)),

$$\lambda_{litho} = -\frac{\Delta\lambda_{CNT}}{2}\left(\frac{C'_{tot}}{C'_{sg}}\right).$$

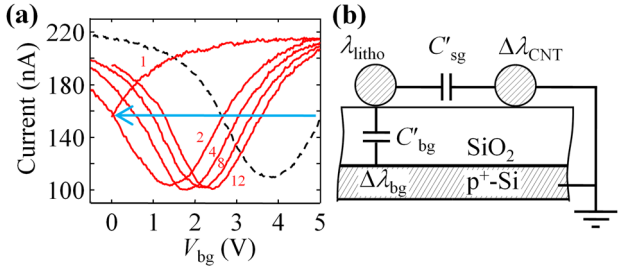

FIG. 4. (Color online) Electrical characteristics before and after writing a uniform charge pattern. (a) The dashed black line shows $I(V_{bg})$ measured at $V_{sd} = 25$ mV before writing charge. The solid red lines show $I(V_{bg})$ at various times after writing charge ($V_{write} = +10$ V). The numbers refer to the number of V_{bg} cycles, for example, curve 4 was obtained on the 4th cycle of sweeping V_{bg}. (b) Equivalent circuit diagram illustrating the capacitive coupling between the lithographic charge, the CNT, and the silicon back gate.

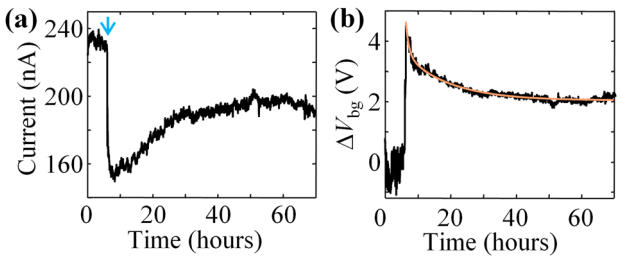

FIG. 5. (Color online) Lifetime of the doping effect. (a) Current measured as a function of time at $V_{bg}=0$ and $V_{sd}=100$ mV. Charge lithography took place at $t\sim6$ h indicated by an arrow ($V_{write}=+10$ V). (b) Data from (a) expressed in terms of ΔV_{bg}. The $I(V_{bg})$ device characteristics were used to calculate the effective change in gate voltage ΔV_{bg}. The fit line is a double exponential decay with half lives of 1 and 14 h.

The factor of 2 arises because two lines of charge were drawn, one on either side of the CNT. We estimate $C'_{sg}\sim14$ aF/μm from the geometric capacitance between two parallel wires of radius $r\sim1.9$ nm, separated by 300 nm and an effective dielectric environment $\varepsilon=2.5$. Additional contributions to C'_{tot} are dominated by the capacitance between the patterned charge and the back gate which we estimate using Eq. (1). We conclude that $\lambda_{litho}\sim2400e$ μm^{-1} when $V_{write}=+10$ V.

For practical applications of charge lithography, the lifetime of the charge pattern is an important consideration. We noted above that sweeping V_{bg} erases doping effects (Fig. 4(a)). If V_{bg} and V_{sd} are kept small ($\sim$100 mV), however, the doping effect persists for many days. Fig. 5(a) shows a long time trace from a CNT FET before and after writing charge. Baseline conductivity was established during the first 6 h. Charge was then written using $V_{write}=+10$ V so that the lithographic side gates uniformly doped the length of the CNT. Over the next 70 h, the conductance tended toward its original value but never fully recovered. EFM measurements taken at $t=70$ h showed no sign of the written charge, and the lingering ΔV_{bg} was erased by sweeping V_{bg}.

The time evolution of ΔV_{bg} follows a bi-exponential decay (Fig. 5(b)). The bi-exponential behavior suggests that two mechanisms are causing ΔV_{bg} to decay. We hypothesize that the faster process corresponds to the build-up of screening charge in the SiO_2 near the CNT, while the slower process corresponds to the dissipation of λ_{litho} into the surrounding environment. Previous authors have verified that charge leaks from electrically connected CNTs into the nearby SiO_2 on a time scale of minutes to hours when radial electric fields are present.[3,17] This charge leaking effect leads to a build-up of charge that would screen the electric field generated by λ_{litho}. Compared to the process of charge leaking, the decay of λ_{litho} should be significantly slower. The patterned charge is located far from any conducting objects so charge must migrate over the oxide surface, or through the oxide, to reach a conducting reservoir. We have used KFM imaging to confirm that λ_{litho} remains localized on the oxide surface for several hours. Regardless of the exact decay mechanisms, the lifetime of the doping effect is long and provides ample time to explore the characteristics of a device with a tailored doping profile. Moreover, we expect that the mechanisms causing ΔV_{bg} to decay can be suppressed, if needed, by cooling the device to cryogenic temperatures.

In conclusion, we have used electrical characterization and scanning probe techniques to investigate the response of CNT FETs to lithographically patterned surface charge. The spatial resolution of the doping modulation is approximately 300 nm (the distance between the charge and CNT) and magnitude of ΔE_F is tunable up to ±1 eV. We have demonstrated a charge pattern that turns a CNT FET into a pn junction. Other simple charge patterns could be used to create devices such as double quantum dots, gradated p-i-n junctions, or FETs with engineered hotspots. We anticipate that the ability to controllably and reversibly modulate the doping profiles in nanoscale electronic and optoelectronic devices will enable a variety of new investigations.

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