- **Inputs Are TTL-Voltage Compatible**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT04 . . . J OR W PACKAGE
SN74AHCT04 . . . D, DB, DGV, N, OR PW PACKAGE
(TOP VIEW)

1A	1	14 V_{CC}
1Y	2	13 6A
2A	3	12 6Y
2Y	4	11 5A
3A	5	10 5Y
3Y	6	9 4A
GND	7	8 4Y

SN54AHCT04 . . . FK PACKAGE
(TOP VIEW)

Top pins: 1Y, 1A, NC, V_{CC}, 6A (pins 3, 2, 1, 20, 19)

2A	4	18 6Y
NC	5	17 NC
2Y	6	16 5A
NC	7	15 NC
3A	8	14 5Y

Bottom pins: 3Y, GND, NC, 4Y, 4A (pins 9, 10, 11, 12, 13)

NC – No internal connection

description

The 'AHCT04 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

The SN54AHCT04 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†
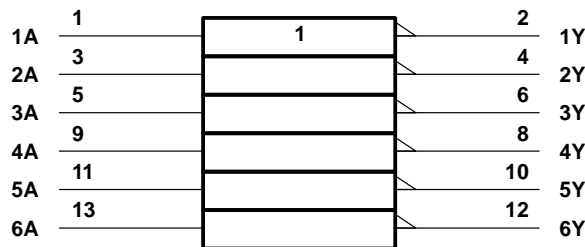
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

Copyright © 1997, Texas Instruments Incorporated

TEXAS INSTRUMENTS

SN54AHCT04, SN74AHCT04
HEX INVERTERS

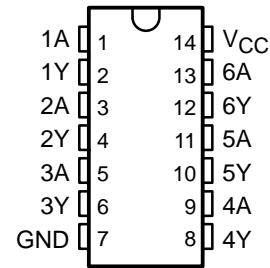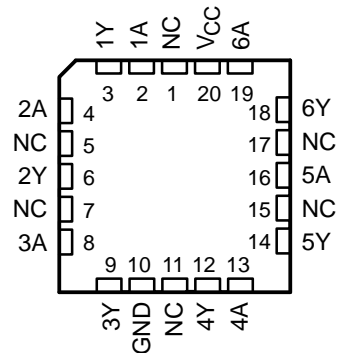SCLS232G – OCTOBER 1995 – REVISED JULY 1997

logic diagram (positive logic)

A ———————▷○——————— Y
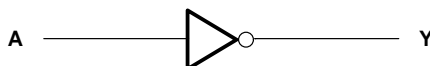
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . −20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . 127°C/W
                                                        DB package . . . . 158°C/W
                                                        DGV package . . . . 182°C/W
                                                        N package . . . . 78°C/W
                                                        PW package . . . . 170°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
         2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT04		SN74AHCT04		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−8		−8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$			SN54AHCT04		SN74AHCT04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu A$		4.5 V	4.4	4.5		4.4		4.4		V
	$I_{OH} = -8\ mA$			3.94			3.8		3.8		
V_{OL}	$I_{OL} = 50\ \mu A$		4.5 V			0.1		0.1		0.1	V
	$I_{OL} = 8\ mA$					0.36		0.44		0.44	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V			2		20		20	μA
$\Delta I_{CC}^\dagger$	One input at 3.4 V, Other inputs at V_{CC} or GND		5.5 V			1.35		1.5		1.5	mA
C_i	$V_I = V_{CC}$ or GND		5 V		4	10				10	pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\ V \pm 0.5\ V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT04					UNIT
				$T_A = 25°C$			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}^*	A	Y	$C_L = 15\ pF$		4.7	6.7	1	7.5	ns
t_{PHL}^*					4.7	6.7	1	7.5	
t_{PLH}	A	Y	$C_L = 50\ pF$		5.5	7.7	1	8.5	ns
t_{PHL}					5.5	7.7	1	8.5	

* On products compliant to MIL-PRF-38535, this parameter is warranted but not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\ V \pm 0.5\ V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT04					UNIT
				$T_A = 25°C$			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	$C_L = 15\ pF$		4.7	6.7	1	7.5	ns
t_{PHL}					4.7	6.7	1	7.5	
t_{PLH}	A	Y	$C_L = 50\ pF$		5.5	7.7	1	8.5	ns
t_{PHL}					5.5	7.7	1	8.5	

noise characteristics, $V_{CC} = 5\ V$, $C_L = 50\ pF$, $T_A = 25°C$ (see Note 4)

PARAMETER		SN74AHCT04			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

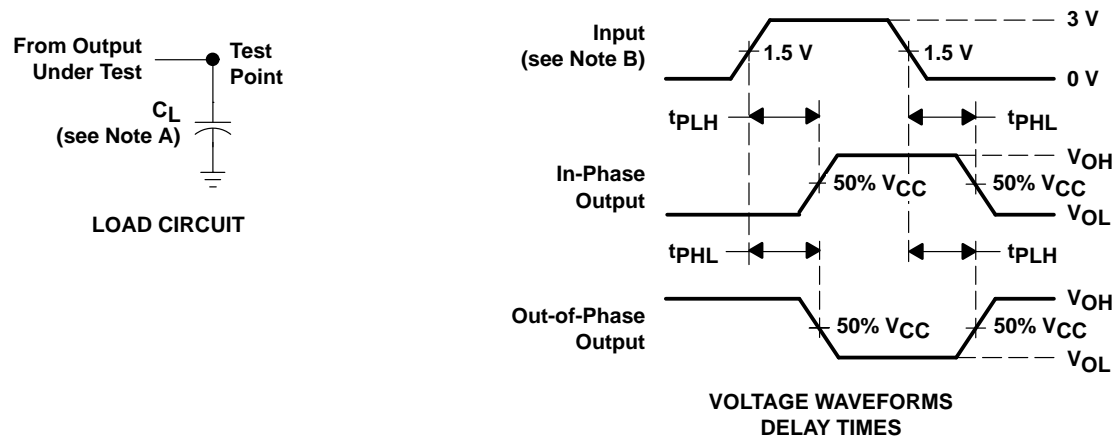NOTE 4: Characteristics are for surface-mount packages only. These parameters are warranted but not production tested.

TEXAS
INSTRUMENTS

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
　　　　 B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
　　　　 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.