125-GHz Diode Frequency Doubler in 0.13-μm CMOS

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***Abstract*—The first mm-wave Schottky diode frequency doubler fabricated in CMOS is demonstrated. The doubler built in 130-nm CMOS uses a balanced topology with two shunt Schottky barrier diodes, and exhibits ~10-dB conversion loss as well as −1.5-dBm output power at 125 GHz. The input matching is better than −10 dB from 61 to 66 GHz. The rejection of fundamental signal at output is greater than 12 dB for input frequency from 61 to 66 GHz. The doubler can generate signals up to 140 GHz.**

***Index Terms*—CMOS, doubler, frequency multiplication, millimeter wave, Schottky barrier diode, terahertz.**

I. Introduction

RECENT advances in CMOS have made implementation of voltage controlled oscillators [1]–[5] and a Schottky diode detector [6] operating above 100 GHz possible. In fact, with the scaling, it appears that terahertz CMOS circuits will be possible [7]–[9]. This will potentially allow implementation of highly integrated THz imaging and spectroscopy systems for scientific, medical, military and commercial applications [10] that may cost hundreds of dollars instead of hundreds of thousands.

A fundamental building block for these systems is a signal source. A common electronic method for signal generation at this frequency range is frequency multiplication using III-V Schottky barrier diodes to translate low frequency signals to higher frequencies [11]–[14]. To date, no multipliers operating at 100 GHz and higher have been demonstrated in CMOS. The only one demonstrated in a main stream silicon technology is the Schottky diode frequency doubler with conversion loss (CL) of ~14 dB at 110 GHz output frequency implemented in a 0.13-μm SiGe BiCMOS technology [15], [16].

Based on the reported CMOS Schottky barrier diode with cut-off frequency higher than 1 THz and breakdown voltage of ~10 V [17], it should be possible to implement a frequency doubler with output frequency above 300 GHz. As a step toward demonstrating such a circuit, this paper presents the design, analyses and measurement results of the first mm-wave Schottky diode frequency doubler fabricated in CMOS, which exhibits ~10-dB conversion loss and −1.5-dBm output power at 125 GHz.

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The paper is organized as follows. Section II describes the topology of frequency doubler. The circuit implementation and design considerations are presented in Section III. Section IV presents the simulated and experimental results. Finally, the paper is summarized in Section V.

II. Frequency Doubler Topology

Fig. 1 shows a cross section and layout of Schottky barrier diodes that are implemented in CMOS technology without any process modifications, where l_s is the unit square-shape Schottky anode length, l_1 is the STI ring width, l_2 is the separation between n-well contact metals and STI edge, and l_3 is the parallel diode unit cell spacing. The Schottky barrier is formed by blocking n^+ implantation in selected diffusion regions [17]–[19]. Compared to the Schottky diodes in SiGe BiCMOS technology [15], [16] and [20], due to the unavailability of an n^+ buried layer, the Schottky diode in CMOS is made to have a smaller unit diode cell area ($0.32\times0.32 \sim 0.64\times0.64\ \mu\mathrm{m}^2$) as compared to 1 $\mu\mathrm{m}^2$ in [15], [16], and larger n^+ cathode contact areas to lower the series resistance [17]. These significantly increase the cathode (n-well) to substrate capacitance (40 fF for a diode with 1.64-$\mu\mathrm{m}^2$ anode area and 5.8-fF Schottky junction capacitance). This in combination with non-negligible substrate resistance makes use of a series topology for frequency multiplication in [15], [16] difficult for CMOS. To overcome this, a balanced topology with two shunt diodes with grounded cathodes [21]–[23] in Fig. 2 which can increase output power is utilized for the CMOS implementation.

The 50-Ω transmission lines are used to match input and output impedance to 50 Ω, while the 72-Ω transmission lines connected between the Schottky diode pair and 50-Ω transmission line transform the average diode capacitance to $\sim$ 50 Ω at fundamental frequency (f_o) for maximum power delivery to the diodes. Quarter wave open stubs at input and output are used to attenuate the second order harmonic and fundamental signals, respectively. Besides these, to minimize conversion loss, unnecessary losses of input signal power in the output networks should be avoided and the same for the output signal power [24]. This can be accomplished by making

$$\mathrm{Re}\,[Y_{do}(f_o)] \approx 0 \text{ and } \mathrm{Re}\,[Y_{di}(2f_o)] \approx 0 \tag{1}$$

where Y_{do} and Y_{di} are conductance seen at node A in Fig. 2 toward load and source, respectively. Since the impedance for the second order harmonics at node B should be approximately zero, the length of L_1 should be a quarter wave at the second harmonic frequency $(2f_o)$. Similarly, the length of L_2 should be close to a quarter wave at the fundamental frequency (f_o). The bond pad parasitics are tuned out by the input and output

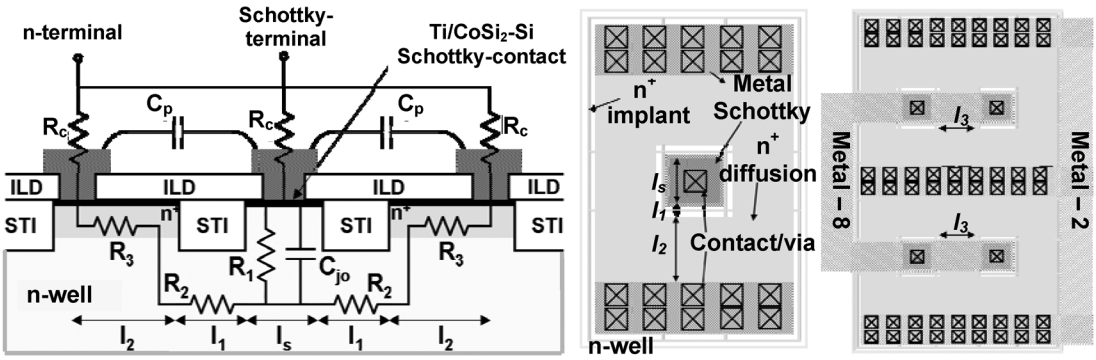


Fig. 1. Schottky diode cross section and layout.

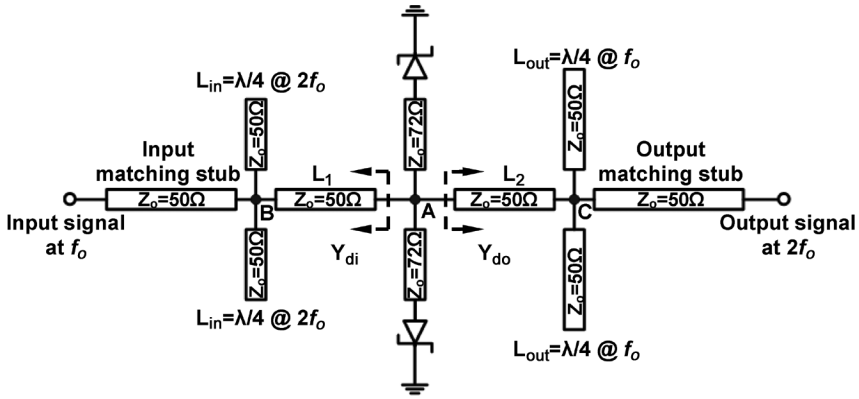


Fig. 2. Frequency doubler schematic.

matching stub, respectively. DC bias of the circuit is applied to the input of the circuit through a 1.2-kΩ on-chip polysilicon resistor.

III. Circuit Implementation

Successful implementation of a diode frequency doubler hinges on proper design and accurate modeling of TL matching networks and the diode at all harmonic frequencies. For the design of a diode frequency doubler in integrated circuit form, proper sizing of diode is an additional consideration. In this section, these design issues are addressed.

A. Schottky Barrier Diode Design

The heart of every frequency multiplier operating higher than 100 GHz is a Schottky diode. The performance of diode determines the intrinsic efficiency (conversion loss), and the maximum output power the multiplier can achieve [25]. Optimizations of both Schottky diode geometry and physical characteristics (doping, epitaxial layer thickness, etc.) have been extensively investigated for III-V diode multiplier designs [25]–[27].

Varactor mode operation of diode which eliminates real power consumption in the junction using only reactive components [28] is chosen in this design to achieve higher conversion efficiency. In this mode, a diode is reverse biased and voltage modulation on the junction capacitance

$$C_j = \frac{C_{jo}}{(1 - V/\phi_{bi})^{m_j}} \tag{2}$$

where C_{jo} is the zero-bias junction capacitance, ϕ_{bi} is the built-in potential and m_j is the junction grading coefficient, causes reactive multiplication.

The junction grading coefficient, m_j is a dominant factor determining the varactor mode conversion efficiency. For Schottky diodes fabricated in CMOS, m_j is degraded by the parasitic capacitance C_p in Fig. 3 between the Schottky contact metal lines and n-well as well as its contact metals [17]. Since a diode with a larger unit cell area requires less interconnections at given capacitance, such a diode will have higher m_j. Fig. 4 shows the measured m_j for multiple square-shape diode test structures, which is consistent with the above discussion.

The series resistance R_s is another critical parameter that strongly influences frequency multiplier performance. It is composed of two components: the real part of undepleted region impedance, and the ohmic contact resistance [24]. This series resistance and zero-bias diode junction capacitance determine the cut-off frequency ($f_c = 1/2\pi R_s C_{jo}$). For Schottky diodes fabricated in CMOS, the analyses in [17] show that the zero-bias junction capacitance C_{jo} is approximately proportional to the diode unit cell area A_s, while R_s is roughly proportional to $A_s^{-0.5}$. These indicate that decreasing A_s will increase the cut-off frequency. However, this will degrade m_j. Thus, m_j and cut-off frequency must be properly traded off.

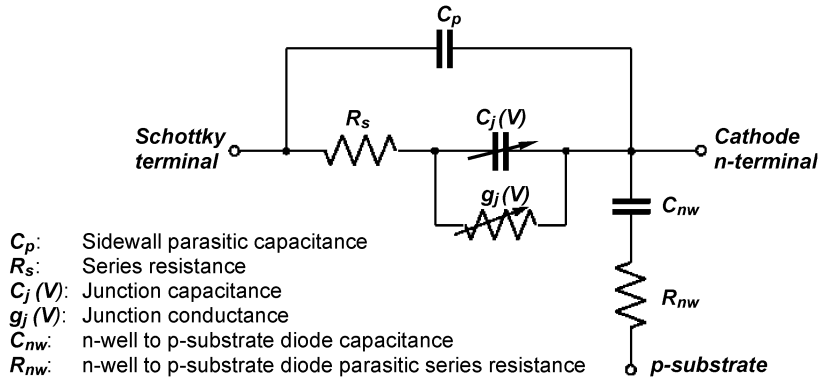


Fig. 3. Schottky barrier diode small signal equivalent model.

TABLE I
A $38 \times 0.64 \times 0.64\ \mu\text{m}^2$ SCHOTTKY BARRIER DIODE CHARACTERISTICS

Series resistance R_s (Ω)	Zero bias junction capacitance C_{jo} (fF)	Saturation current I_s (nA)	Grading coefficient m_j	Ideality factor η	Cut-off frequency f_c (GHz)
4.7	50	4.75	0.49	1.03	680

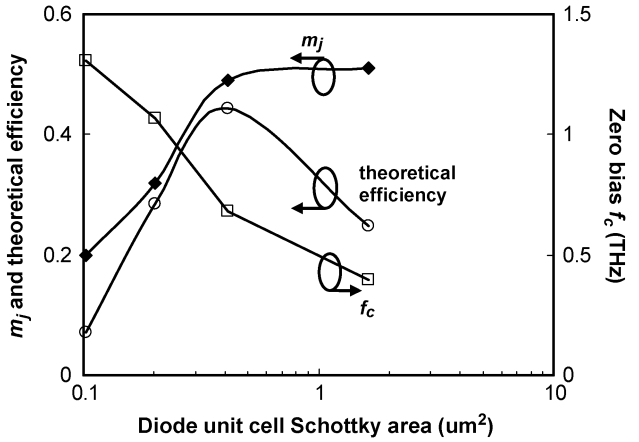


Fig. 4. Measurement results of m_j and cut-off frequency for Schottky diodes with varying unit cell area. Theoretical efficiency calculated using equation (3) is also shown.

According to [29], for a fully-driven diode operating in the varactor mode (voltage swing across diode is from breakdown to turn-on voltage), the maximum conversion efficiency of the diode is

$$\eta = \frac{1 - B(m_j)\frac{\omega}{\omega_c^*}}{1 + B(m_j)\frac{\omega}{\omega_c^*}} \tag{3}$$

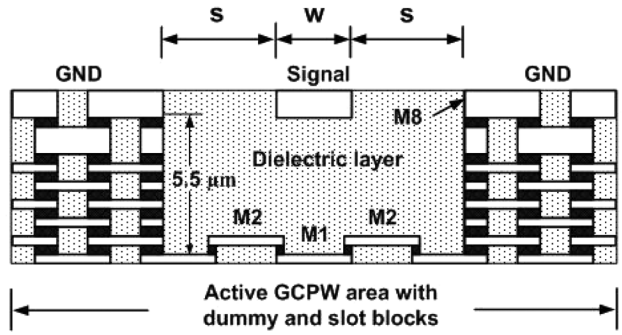
where ω_c^* is the cut-off frequency at breakdown voltage of the diode, ω is the fundamental frequency. $B(m_j)$ is a monotonically decreasing function of m_j for its value less than 0.6, which is the case for the integrated Schottky diode structure. The calculated theoretical efficiency based on (3) is also shown in Fig. 4. Based on this, the diode unit cell area A_s was set to $0.64\ \mu\text{m} \times 0.64\ \mu\text{m}$ with optimized dimension of $l_1 = 0.22\ \mu\text{m}$, $l_2 = 1\ \mu\text{m}$ and $l_3 = 0.6\ \mu\text{m}$ in Fig. 1 [17]. To reduce the parasitic capacitance, top metal layer (metal 8) is used to connect the anodes of unit diode cells, while the n-well contact is formed by shunting the two lowest metal layers. Table I lists the measured parameters for a $38 \times 0.64\ \mu\text{m} \times 0.64\ \mu\text{m}$ diode.

B. Transmission Line Design

Grounded coplanar waveguide (GCPW) is used in this design for its low loss, good isolation to and from other circuits as well as compatibility for ground-signal-ground probing at millimeter-wave frequencies [30]–[32]. As shown in Fig. 5, the signal and two ground conductors are formed with the top metal layer, and the ground conductors are connected to the ground plane formed by metal 1 and 2 layers through vias [33], [34] to satisfy the metal width rule with dummy blocks.

To match 50-Ω input and output, a 50-Ω GCPW was implemented. For the transmission lines connecting to the diode pair, higher characteristic impedance is desired. A higher Z_o line is more inductive at given length so that a shorter transmission line with lower total loss can be used to tune out the capacitance of the diodes. This increases the voltage swing seen by the diode which typically increases the conversion efficiency. However, if the total width of GCPW $(2s + w)$ is fixed to keep the area constant, a high Z_o transmission line has higher loss due to the narrower signal conductor required [35]. For proper optimization, transmission lines with varying ratios between ground and signal conductor spacing (s), and signal conductor width (w) were simulated in a 3-D E-M simulator, High Frequency Structural Simulator (HFSS). The total width of GCPW was set at 40 μm in simulation. The effective thickness of dielectric layer between the signal line and ground plane is $\sim 5\ \mu$m. A GCPW with $w = 10\ \mu$m and $s = 15\ \mu$m is chosen for the 50-Ω transmission line.

The transmission lines as well as diodes with a varying number of cells were co-simulated in Agilent Advance Design System (ADS) to determine the optimum structure for the high characteristic transmission line. The GCPW with $w = 4\ \mu$m and $s = 18\ \mu\text{m}$ ($Z_o = 72\ \Omega$) resulted the maximum conversion efficiency, thus this structure was chosen for the high characteristic impedance line connecting the diode pairs. The simulated



Z_o	S	W
50 Ω	15μm	10μm
72 Ω	18μm	4μm

Fig. 5. Grounded coplanar waveguide (GCPW) cross section.

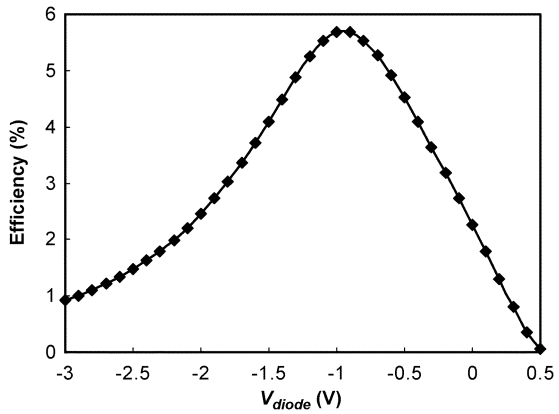


Fig. 6. Simulated efficiency versus diode bias, $\mathrm{V_{diode}}$ for 70-GHz input signal at 10-dBm input power level.

losses for the 50 and 72-Ω transmission lines are ∼0.9 and 1.0 dB/mm at 62.5 GHz and ∼1.5 and 1.6 dB/mm at 125 GHz. To make the layout more compact, the open stubs at the output are folded. The folded structure has been simulated once again in HFSS. The folding increases conversion loss of the circuit at 125 GHz output by only 0.2 dB at 10-dBm input power level.

C. Circuit Bias Condition and Diode Sizing

Using the diode models extracted from measurements and HFSS simulations of transmission lines, harmonic balance and S-parameter simulations were performed in ADS to determine the optimum diode size and transmission line lengths as well as the proper DC bias for the diode.

Input power level and m_j determine the bias point and diode size for the maximum efficiency. For the optimized diode structure in this varactor mode design with a unit cell area of $0.64\ \mu\mathrm{m} \times 0.64\ \mu\mathrm{m}$ and $m_j = 0.49$, the optimum bias for $P_{\mathrm{in}} = 10$ dBm and $f_{\mathrm{in}} = 70$ GHz is -1 V, and the simulated maximum efficiency is 5.7%. The voltage across the diode varies from 0 V to -3.9 V and the diode is mostly in varactor mode. Fig. 6 shows the simulated efficiency dependence on diode bias. The efficiency improves from around 2% at zero diode bias. When the reverse bias is more positive than the optimum, the efficiency is limited by the clamping action of the forward biased junction while the efficiency is lowered by decreased voltage dependence of capacitance when the reverse bias is more negative than the optimum.

The optimum diode size depends on the input power level, which has been analyzed in [29]. For a fully pumped diode with the voltage swinging from the breakdown voltage to turn-on voltage,

$$P_{avg} = A(m_j)\omega_{\mathrm{in}}C_{\mathrm{min}}(V_{BV} + \phi_{bi})^2 \tag{4}$$

where P_{avg} is the average converted power from the fundamental signal to the second harmonic. Ideally, P_{avg} is equal to input power assuming no loss and optimum matching. $A(m_j)$ is a function of grading coefficient m_j, ω_{in} is fundamental frequency in radian, C_{min} is the minimum capacitance at breakdown voltage, and V_{BV} is the breakdown voltage. From (4), as the maximum input handling power level goes up, C_{min} needs to become bigger, which requires a larger diode area. If a diode size is too small, the maximum output power is limited. If a diode size is too big, the required length of high impedance (72-Ω) transmission lines becomes longer and loss increases. Additionally, the lower impedance of a larger diode makes the impact of loss even greater. These will decrease the voltage swing across the diodes, which lead to reduced modulation of junction capacitance and lower efficiency. The simulated optimum size of diode for handling input power of 10 dBm is $\sim$ 16 $\mu\mathrm{m}^2$ or $38 \times 0.64 \times 0.64\ \mu\mathrm{m}^2$ with zero-bias junction capacitance (C_{jo}) of 50 fF and series resistance (R_s) of 4.7 Ω.

IV. Measurement Results

The frequency doubler was fabricated in the UMC 130-nm logic CMOS technology without any process modifications. A photograph of the fabricated chip and the diode array are shown in Fig. 7. The total die area is $\sim$ 1.1 mm × 0.7 mm. The active area including those of the diode and main transmission lines is 0.21 mm^2. Most of the area is occupied by the ground plane formed by shunting metal 1 up to metal 8 layers.

The S-parameters of doubler were measured using an Agilent E8361A network analyzer. A pair of GGB 110H-GSG-150P probes was used to measure the doubler from 40 to 110 GHz. Measurements above 110 GHz are not available because the maximum operating frequency of network analyzer is limited to 110 GHz. Fig. 8 shows the simulated and measured $|\mathrm{S_{11}}|$ and $|\mathrm{S_{22}}|$ at -1.5 V bias for the diode. The measured and simulated behaviors agree well. Input matching $|\mathrm{S_{11}}|$ is below -10 dB between 61 and 66 GHz, while the isolation of fundamental signal at the output $1/|\mathrm{S_{21}}|$ is greater than 12 dB from 61 to 66 GHz.

A power measurement set up shown in Fig. 9 was constructed to measure the output harmonics of the doubler. The input signal from the Agilent E8361 network analyzer is amplified by two Terabeam HMPAV-071 V-band power amplifiers and then fed

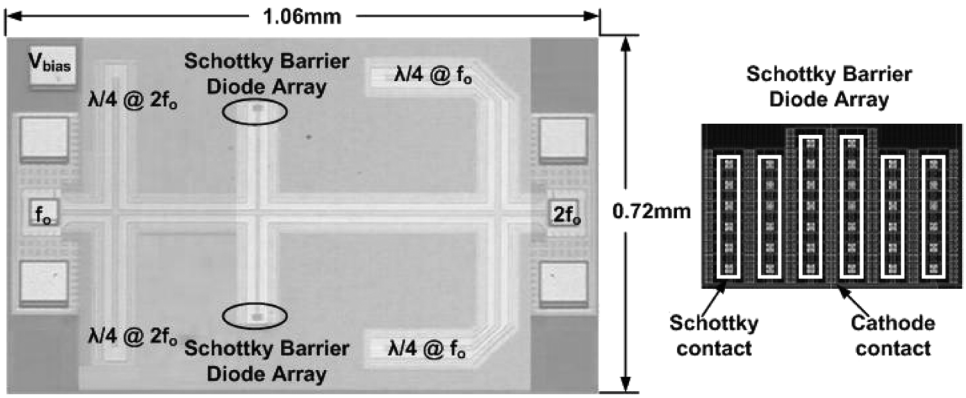


Fig. 7. Die photograph of frequency doubler.

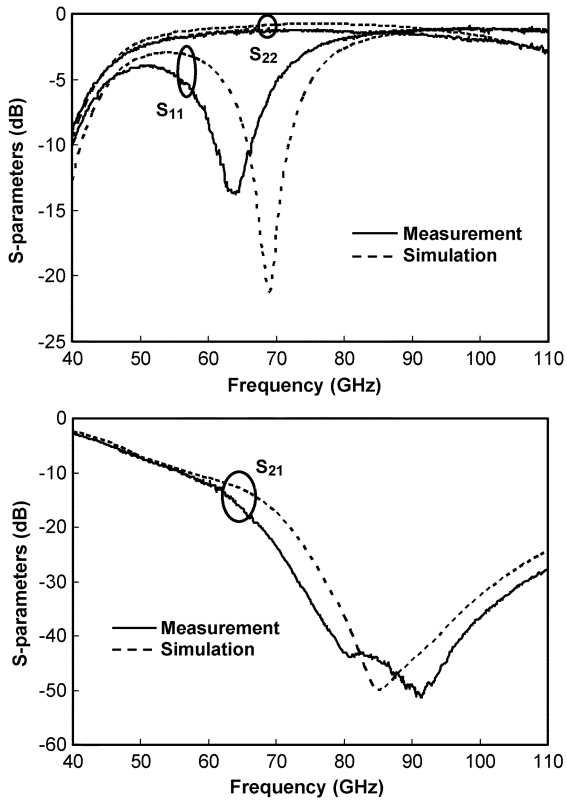


Fig. 8. Measured and simulated S-parameters at $\mathrm{V_{bias}} = -1.5$ V.

to the doubler through a GGB 67A-GS-150P probe. Meanwhile, a GGB 120-GHz ground-signal waveguide probe was used to connect the output to a HP 8563E spectrum analyzer through an Agilent 75 $\sim$ 110-GHz harmonic mixer. The gain of input chain including cables and power amplifiers as well as input probe has been calibrated in 50-Ω system from 55 to 65 GHz for varying power levels using an OML M15HWD 50 $\sim$ 75-GHz harmonic mixer and an HP 8563E spectrum analyzer with the aid of a through structure. The removal of the cable and adaptor technique was employed. The variation of multiple calibrations is less than $\pm$1.5 dB at each frequency point. Due to the power limitation of the power amplifier, the maximum calibrated power that can be provided to the frequency doubler is 8.5 dBm at frequencies between 55 and 63 GHz.

The frequency response of Agilent 75 $\sim$ 110-GHz harmonic mixer has been characterized with an ELVA-1 75 $\sim$ 110 GHz power meter and a HP 8563E spectrum analyzer from 75 to 110 GHz. The loss of mixer from 110 to 125 GHz was linearly extrapolated from the measured data. The calibrated as well as extrapolated loss is shown in Fig. 10. The variation of harmonic mixer loss measurements over multiple calibrations is less than $\pm$1.2 dB at each frequency point. At 125 GHz the estimated loss is $\sim$3.8 dB higher than that measured at 110 GHz. In reality, the loss will be even higher due to propagation of multiple modes in the waveguide of harmonic mixer above 110 GHz [36]. The output probe loss was assumed to be the same as that at 110 GHz ($\sim$1.6 dB from the data sheet). Once again, the actual loss is expected to be higher. Thus, the de-embedded power and conversion gain are under estimated.

The diodes are biased by an external power supply through the 1.2-kΩ on-chip non-silicide polysilicon resistor. The optimum bias voltage for each diode is around -2 V for 8.5-dBm pump power at 125-GHz output. The DC bias current in each diode is 3 μA. Using the frequency extension module of network analyzer, the frequency of input signal was swept up to 75 GHz at input power level of $\sim$8 dBm. Outputs at frequencies up to 140 GHz have been observed.

Fig. 11 shows the conversion loss (CL) and output power versus the output frequency for three different input power levels. The maximum output power and minimum CL occur around 125 GHz. The ringing in the CL plots is most likely due to the variation of PA matching (Fig. 9) with frequency. The measured CL and output power versus input power at 125 GHz output are shown in Fig. 12. Once again the measured and simulated behaviors agree reasonably. The difference between simulation and measurement is likely due to the errors of diode and transmission line modeling as well as measurement uncertainties. The minimum CL of about 10 dB occurs at input power of 8.5 dBm, corresponding to $\sim$10% efficiency. The maximum output power is ~ -1.5 dBm at 125 GHz. There is no saturation of CL up to input power of 8.5 dBm suggesting that the doubler should be able to provide even higher output

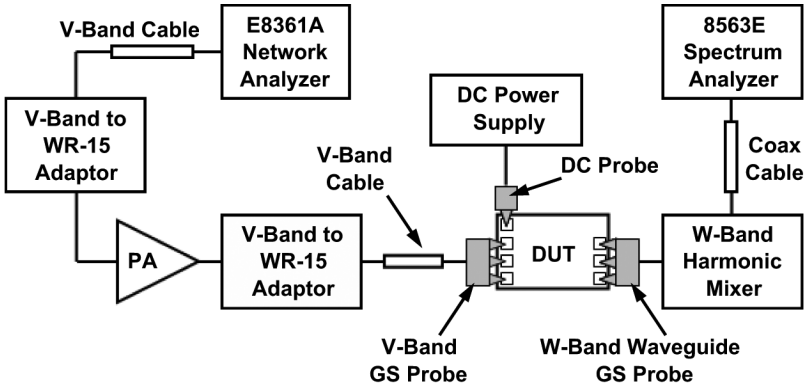


Fig. 9. Power measurement setup.

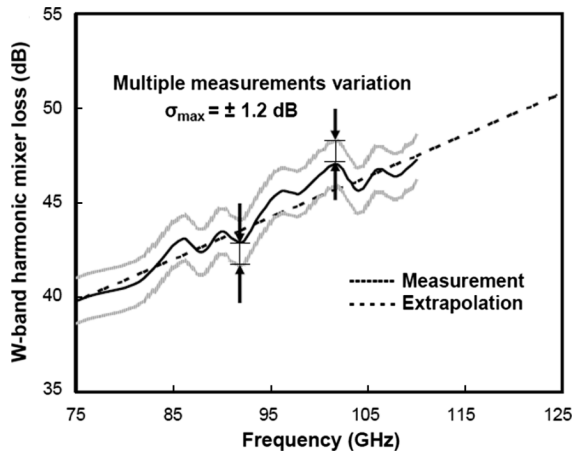


Fig. 10. Agilent 75 ∼ 110-GHz harmonic mixer loss calibration and extrapolation.

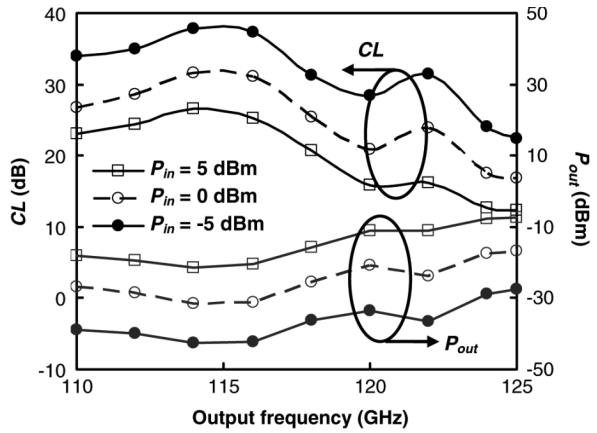


Fig. 11. Conversion loss and $\mathrm{P_{out}}$ versus output frequency at $\mathrm{V_{bias}} = -1.5\ \mathrm{V}$.

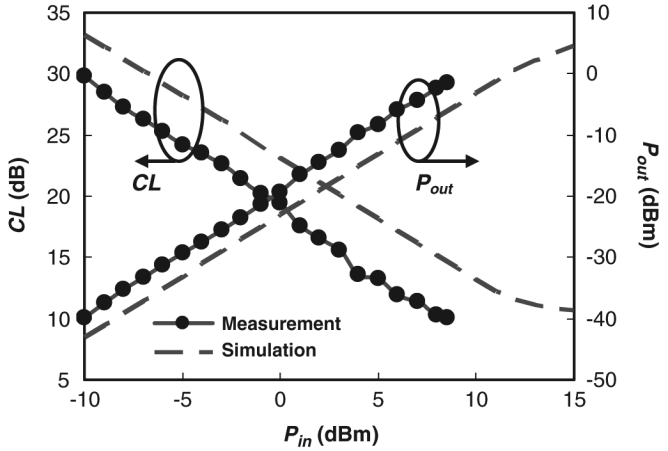


Fig. 12. Conversion loss and $\mathrm{P_{out}}$ versus input power for 125-GHz output at $\mathrm{V_{bias}} = -2\ \mathrm{V}$. Simulation results for $\mathrm{V_{bias}} = -2$ are also shown.

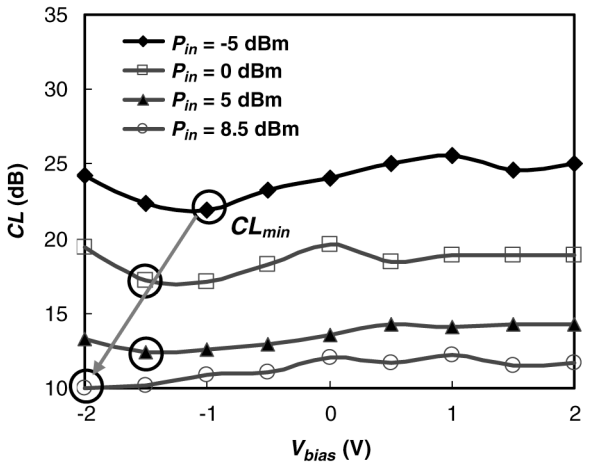


Fig. 13. Conversion loss versus bias for 125-GHz output at varying input power levels.

power if an input signal source with higher calibrated power is used.

Fig. 13 shows the bias dependence of the conversion loss for 125-GHz output signal. $\mathrm{V_{bias}}$ is the bias voltage applied at the DC pad. This is essentially the DC voltage across the diode when it is reverse biased. As discussed, with the increasing input power level, the optimum bias point of conversion loss shifts more negative to avoid the compression resulting from forward conduction of the diode. The performance of frequency doubler is summarized in Table II.

V. Conclusion

A millimeter-wave Schottky diode frequency doubler built in digital CMOS technology is demonstrated for the first time.

TABLE II
PERFORMANCE SUMMARY

	Frequency doubler in [21]	Frequency doubler in [15], [16]	This work
Topology	Shunt type	Series type	Shunt type
Nonlinear device	Schottky barrier diode	Schottky barrier diode	Schottky barrier diode
Diode cut-off frequency	~0.6 THz	~1 THz	~0.7 THz
Diode size	66 μm^2 for each diode	4 μm^2	16 μm^2 for each diode
$\|S_{11}\|$ < -10 dB	N/A	50 ~ 55 GHz	61 ~ 66 GHz
Output frequency	70 ~ 76 GHz	95 ~ 110 GHz	110 ~ 125 GHz
Bias voltage	Negative bias	0 V	-2 V
Minimum conversion loss	4.4 dB @ f_{out} = 76 GHz	~ 12 dB @ f_{out} =100 GHz	10 dB @ f_{out} =125 GHz
Maximum output power	15.6 dBm @ f_{out} =76 GHz, P_{in} = 20 dBm	2.5 dBm @ f_{out} =100 GHz, P_{in} = 16 dBm	-1.5 dBm @ f_{out} =125 GHz, P_{in} = 8.5 dBm
Technology	GaAs	0.13-µm SiGe BiCMOS	0.13-µm CMOS

Conversion loss of ~10 dB at 125-GHz output frequency is comparable to that of the doubler fabricated with the Schottky diode using an n^+ buried layer in the SiGe BiCMOS process at 100 GHz [15], [16]. This is due to the varactor operation of CMOS doubler instead of the combination of varactor and varistor mode operation of the doubler in [15], [16], and optimization of Schottky diode m_j and cut-off frequency for the varactor mode operation of CMOS doubler. The maximum output power of the diode doubler is greater than -1.5 dBm. Using the Schottky barrier diodes, it should be possible to implement frequency doublers operating above 300 GHz, albeit at lower conversion efficiency and output power. This work provides additional support for the possibility of using CMOS technology to build systems operating in the upper millimeter-wave and terahertz regions.

REFERENCES

[1] R.-C. Liu, H.-Y. Chang, C.-H. Wang, and H. Wang, "A 63 GHz VCO using a standard 0.25 μm CMOS process," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2004, pp. 446–447.

[2] C. Cao, E. Seok, and K. K. O, "192-GHz push-push VCO in 0.13- μm CMOS," *Electron. Lett.*, vol. 42, pp. 208–210, Feb. 2006.

[3] C. Cao and K. K. O, "A 140-GHz fundamental mode voltage-controlled oscillator in 90-nm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, pp. 555–557, Oct. 2006.

[4] P.-C. Huang, M.-D. Tsai, H. Wang, C.-H. Chen, and C.-S. Chang, "A 114 GHz VCO in 0.13 μm CMOS technology," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2005, pp. 404–405.

[5] L. M. Franca-Neto, R. E. Bishop, and B. A. Bloechel, "60 GHz and 100 GHz VCOs in 90 nm CMOS using optimum pumping method," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2004, pp. 444–445.

[6] E. Seok, C. Cao, S. Sankaran, and K. K. O, "A millimeter-wave schottky diode detector in 130-nm CMOS technology," in *Symp. VLSI Circuits Dig.*, Jun. 2006, pp. 178–179.

[7] E. Y. Seok, C. Cao, D. Shim, D. J. Arenas, D. Tanner, C.-M. Hung, and K. K. O, "410-GHz CMOS push-push oscillator with a patch antenna," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 472–473.

[8] K. K. O, C. Cao, E.-Y. Seok, and S. Sankaran, "100–200 GHz CMOS signal sources and detectors," in *Proc. Compound Semiconductor IC Symp.*, Portland, OR, Oct. 2007, pp. 1–4.

[9] D. Huang, T. R. LaRocca, L. Samoska, A. Fung, and M.-C. F. Chang, "324 GHz CMOS frequency generator using linear superposition technique," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 476–477.

[10] T. Crowe, W. L. Bishop, D. W. Porterfield, J. L. Hesler, and R. M. Weikle, "Opening the Terahertz window with integrated diode circuits," *IEEE J. Solid-State Circuits*, vol. 40, no. 10, pp. 2104–2110, Oct. 2005.

[11] G. Chattopadhyay, E. Schlecht, J. Gill, S. Martin, A. Maestrini, D. Pukala, F. Maiwald, and I. Mehdi, "A broadband 800 GHz Schottky balanced doubler," *IEEE Microw. Wireless Compon. Lett.*, vol. 12, no. 4, pp. 117–118, Apr. 2002.

[12] B. Schumann and R. Judaschke, "A five-element 150/300 GHz frequency doubler," in *Infrared and Millimeter Waves Conf. Dig.*, Sep. 2002, pp. 131–132.

[13] D. W. Porterfield, T. W. Crowe, R. F. Bradley, and N. R. Erickson, "A high-power fixed-tuned millimeter-wave balanced frequency doubler," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 4, pp. 419–425, Apr. 1999.

[14] N. Erickson, "High efficiency submillimeter frequency multipliers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1990, pp. 1301–1304.

[15] C. Mishra, U. Pferffer, R. Rassel, and S. Reynolds, "Silicon Schottky diode power converters beyond 100 GHz," in *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, Jun. 2007, pp. 547–550.

[16] U. R. Pferiffer, C. Mishra, R. M. Rassel, S. Pinkett, and S. K. Reynolds, "Schottky barrier diode circuits in silicon for future millimeter-wave and Terahertz applications," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 2, pp. 364–371, Feb. 2008.

[17] S. Sankaran and K. K. O, "Schottky barrier diodes for millimeter wave detection in a foundry CMOS process," *IEEE Electron Device Lett.*, vol. 26, pp. 492–494, Jul. 2005.

[18] F.-J. Huang and K. K. O, "Metal-oxide semiconductor field-effect transistors using Schottky Barrier Drains (SBDR)," *Electron. Lett.*, vol. 33, no. 33, pp. 1341–1342, Jul. 1997.

[19] F.-J. Huang and K. K. O, "Schottky clamped nMOS transistors implemented in a conventional 0.8-μm CMOS process," *IEEE Electron Device Lett.*, vol. 19, no. 9, pp. 326–328, Sep. 1998.

[20] R. M. Rassel, J. B. Johnson, B. A. Orner, S. K. Reynolds, M. E. Dahlstrom, J. S. Rascoe, A. J. Joseph, B. P. Gaucher, J. S. Dunn, and S. A. St. Onge, "Schottky barrier diodes for millimeter wave SiGe BiCMOS applications," in *Proc. Bipolar/BiCMOS Circuits and Technology Meeting*, Oct. 2006.

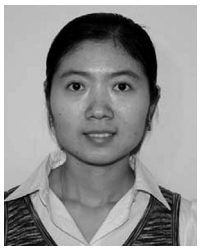
[21] Y. Lee, J. R. East, and L. P. B. Katehi, "High efficiency W-band GaAs monolithic frequency multipliers," *IEEE Trans. Microw. Theory Tech.*, vol. 52, pp. 529–535, Feb. 2004.

[22] J. Papapolymerou, F. Brauchler, J. East, and L. P. B. Katehi, "W-band finite ground coplanar monolithic multipliers," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 5, pp. 614–619, May 1999.

[23] F. Brauchler, J. Papapolymerou, J. East, and L. Katehi, "W-band monolithic multipliers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Jun. 1997, pp. 1641–1644.

[24] M. T. Faber, J. Chramiec, and M. E. Adamski, *Microwave and Millimeter-Wave Diode Frequency Multipliers*. Boston, MA: Artech House, 1995.

[25] S.-W. Chen, T. C. Ho, and P. D. Rice, "Rigorous analysis and design of a high-performance 94 GHz MMIC doubler," *IEEE Trans. Microw. Theory Tech.*, vol. 41, no. 12, pp. 2317–2322, Dec. 1993.
[26] J. Bruston, R. P. Smith, I. Mehdi, P. H. Siegel, and P. Encrenaz, "Analysis and optimization of planar rectangular T-anode Schottky barrier diodes for submillimeter-wave multipliers," in *Proc. 26th European Microwave Conf.*, Oct. 1996, vol. 1, pp. 300–304.
[27] B. J. Rizzi, T. W. Crowe, and N. R. Erickson, "A high-power millimeter-wave frequency doubler using a planar diode array," *IEEE Micow. Guided Wave Lett.*, vol. 3, no. 6, pp. 188–190, Jun. 1993.
[28] A. V. Raisanen, "Frequency multipliers for millimeter and submillimeter wavelengths," *Proc. IEEE*, vol. 80, no. 11, pp. 1842–1852, Nov. 1992.
[29] T. C. Leonard, "Prediction of power and efficiency of frequency doublers using varactors exhibiting a general nonlinearity," *Proc. IEEE*, pp. 1135–1139, Aug. 1963.
[30] C. H. Doan, S. Emami, D. A. Sobel, A. M. Niknejad, and R. W. Brodersen, "Design considerations for 60 GHz CMOS radios," *IEEE Commun. Mag.*, vol. 42, no. 12, pp. 132–140, Dec. 2004.
[31] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Design of CMOS for 60 GHz applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2004, pp. 440–538.
[32] V. Radisic, M. Micovic, M. Hu, P. Janke, C. Ngo, L. Nguyen, L. Samoska, and M. Morgan, "164-GHz MMIC HEMT doubler," *IEEE Microw. Wireless Compon. Lett.*, vol. 11, no. 6, pp. 241–243, Jun. 2001.
[33] K. Jaewon, B. Jung, P. Cheung, and R. Harjani, "Novel CMOS low-loss transmission line structure," in *Proc. IEEE Radio and Wireless Conf.*, Sep. 2004, pp. 235–238.
[34] B. Kleveland, C. H. Diaz, D. Vook, L. Madden, T. H. Lee, and S. S. Wong, "Exploiting CMOS reverse interconnect scaling in multigigahertz amplifier and oscillator design," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1480–1488, Oct. 2001.
[35] C. Schollhorn, W. Zhao, M. Morschbach, and E. Kasper, "Attenuation mechanisms of aluminum millimeter-wave coplanar waveguides on silicon," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 740–746, Mar. 2003.
[36] D. M. Pozar, *Microwave Engineering*, 2nd ed. Reading, MA: Addison-Wesley, 1998, pp. 120–132.



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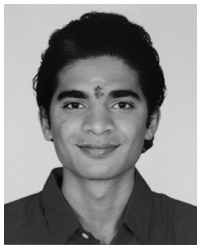

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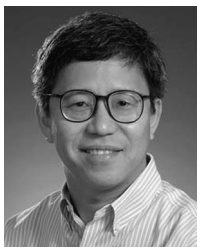

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