A 60-GHz CMOS Receiver Front-End

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***Abstract*—The unlicensed band around 60 GHz can be utilized for wireless communications at data rates of several gigabits per second. This paper describes a receiver front-end that incorporates a folded microstrip geometry to create resonance at 60 GHz in a common-gate LNA and active mixers. Realized in 0.13-μm CMOS technology, the receiver front-end provides a voltage gain of 28 dB with a noise figure of 12.5 dB while consuming 9 mW from a 1.2-V supply.**

***Index Terms*—LNAs, millimeter wave circuits, mixers, RF CMOS, transceivers, transmission lines, 60-GHz band.**

I. Introduction

THE 7-GHz unlicensed band around 60 GHz offers the possibility of data communication at rates of several gigabits per second. In addition to satisfying speed-intensive applications, such high data rates can also *reduce* the energy dissipated per bit because the power consumption of RF transceivers has historically increased sublinearly with the data rate. Moreover, the millimeter wavelength permits the integration of multiple antennas on one chip, requiring multiple transceivers and hence high levels of integration.

This paper describes the design of a 60-GHz receiver front-end implemented in 0.13-μm CMOS technology. Device and circuit techniques are presented that overcome the limited speed of the transistors while achieving a low power dissipation. Section II justifies the use of CMOS technology at 60 GHz and Section III describes the receiver architecture. Section IV presents the "folded microstrip" structure and Section V the design of the building blocks. The experimental results are summarized in Section VI.

II. CMOS Technology at 60 GHz

The speed of analog CMOS circuits climbs by roughly one order of magnitude every ten years. For example, the first 1.4-GHz MOS voltage-controlled oscillator (VCO) was reported in 1988 [1], the first 10-GHz CMOS oscillator in 1999 [2], and the first 104-GHz CMOS VCO in 2004 [3]. Also, CMOS amplifiers operating at tens of gigahertz have been demonstrated, e.g., [4]. Given that RF CMOS transceivers approached 1-GHz carrier frequencies in the mid-1990s and 5-GHz carrier frequencies around 2000, it is plausible to assume that CMOS technology is poised to enter the millimeter-wave regime, specifically, the 60-GHz band, in the next few years. This trend is also likely to continue toward the 75-GHz band for automotive radar applications.

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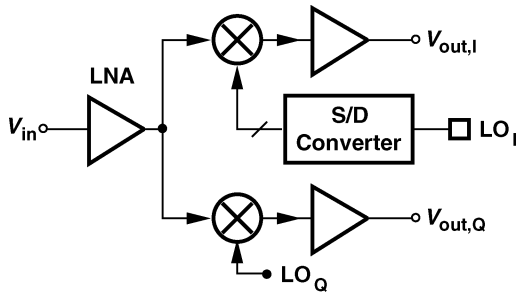

Fig. 1. Receiver architecture.

High-performance 60-GHz transceivers are expected to entail high levels of complexity—greater than today's wireless local area network (WLAN) systems. Multipath issues at high data rates may require orthogonal frequency division multiplexing (OFDM). Moreover, limitations arising from line-of-sight communications and oxygen absorption can be mitigated through the use of beam forming by means of multiple antennas and transceivers. In addition, the large fractional bandwidth (11%) may necessitate multiple staggered high-Q signal paths and several oscillators and even divider chains. For these reasons, CMOS technology appears well suited to the integration of 60-GHz systems—provided an adequate performance can be achieved. For example, [5] reports a 60-GHz CMOS amplifier exhibiting a noise figure of 8.8 dB with a power dissipation of 54 mW.

III. Receiver Architecture

Fig. 1 shows the receiver architecture. The circuit consists of a low-noise amplifier (LNA), quadrature mixers, and baseband gain stages. Since it is extremely difficult to externally generate and distribute differential local oscillator (LO) signals, a single-ended-to-differential (S/D) converter (balun) is included on-chip. The port LO_Q is terminated but not driven, i.e., the lower mixer simply loads the LNA but provides no additional information in this implementation.[1]

To obtain a target for the receiver noise figure, we note that the IEEE 802.16 standard stipulates operation at frequencies as high as 60 GHz with a maximum channel bandwidth of 28 MHz for a data rate of 134 Mb/s and a sensitivity of -65 dBm [6]. This requirement translates to a noise figure of 12 dB. Gigabit-per-second data rates, on the other hand, will necessitate multiple antennas and transceivers to achieve such sensitivities.

With an nMOS f_T of about 75 GHz in 0.13-μm technology, the receiver would suffer from poor performance unless passive resonant devices were exploited in the design. (In principle, if

[1]At these frequencies, quadrature operation is meaningful only if two mixers are driven by on-chip LO phases. Thus, no attempt is made to apply external quadrature LO signals.

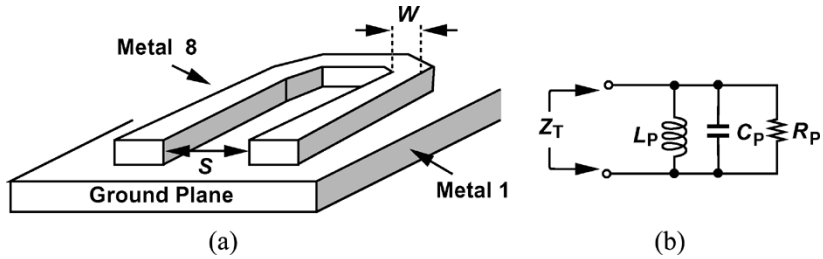

Fig. 2. (a) Folded microstrip and (b) its narrowband equivalent circuit.

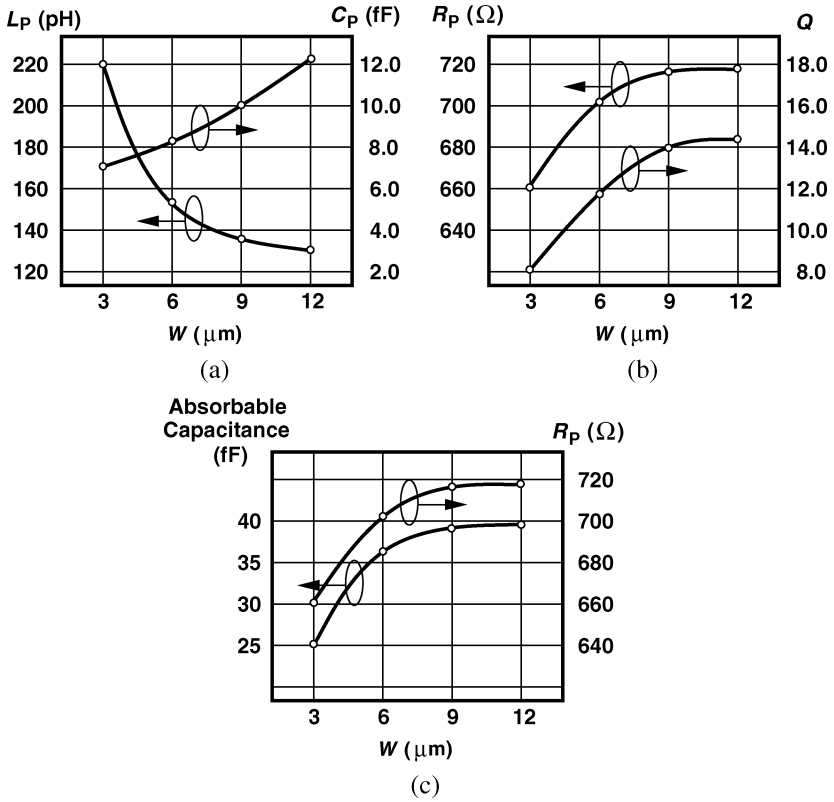

Fig. 3. Dependence of folded microstrip parameters upon linewidth: (a) inductance and capacitance; (b) parallel resistance and Q; (c) maximum absorbable capacitance and parallel resisance.

C_{GS} resonates with an inductor having a quality factor of Q, then the f_T rises by the same factor.) While spiral inductors have proved useful at tens of gigahertz, their performance at 60 GHz may be inadequate due to substrate eddy currents. Such currents equivalently introduce a resistance, R_P, in parallel with the inductor, thereby limiting the $Q\,(= R_P/L\omega)$ at high frequencies. More importantly, the magnetic coupling to the substrate significantly alters the inductance value at these frequencies, requiring detailed knowledge of the substrate profile if an accurate model is to be developed.

In contrast to spiral inductors, transmission lines (T-lines) substantially confine the electric and magnetic fields and hence better lend themselves to modeling. For example, T-lines exhibit a Q relatively independent of the length and hence the inductance value, whereas spiral geometries do not. Nevertheless, the necessary length of such lines (several hundred microns) leads to disproportionately tall layouts, making the routing of the signal and power lines difficult.

Coplanar lines in CMOS technology, introduced in [2], have been characterized for frequencies up to 50 GHz [5]. This work incorporates microstrip structures as they interact negligibly with the substrate and can be modeled more accurately.

IV. Folded Microstrip

In order to alleviate routing difficulties, this design incorporates a "folded" microstrip geometry. Shown in Fig. 2(a), the structure is realized as a metal 8 signal line over a metal 1 ground plane. With the two ends of the line near each other, the layout of the receiver is greatly simplified. (A somewhat similar topology has been used in [7].)

For circuit design, the structure is modeled by the lumped tank depicted in Fig. 2(b), a justified approximation because the total length of the line is about one-tenth of the wavelength.[2]

[2]Under this condition, the structure can be tuned by means of varactors to accomodate a greater bandwith.

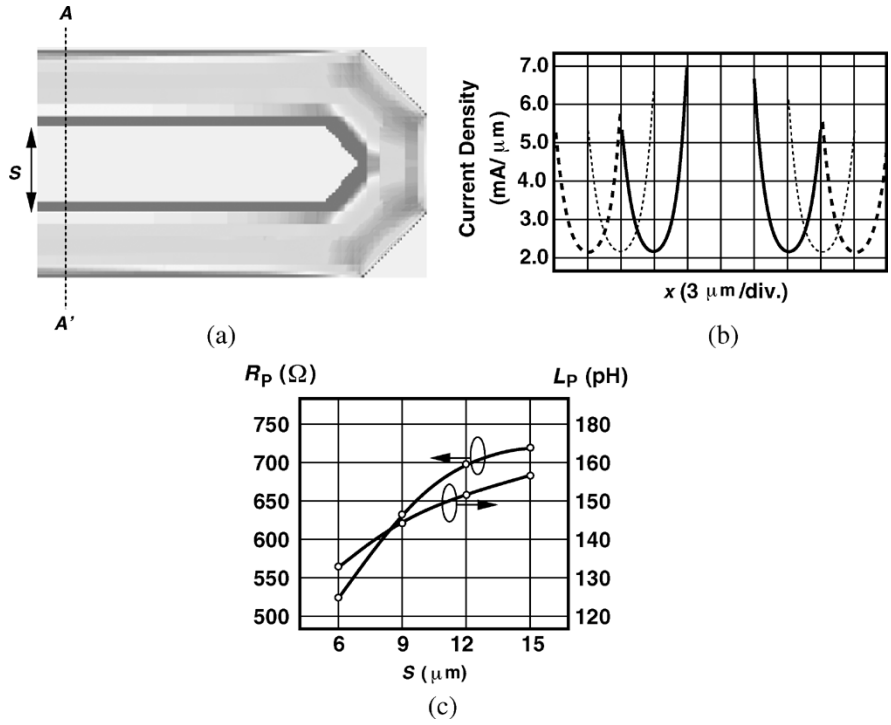

Fig. 4. (a) Example of current distribution in folded microstrip. (b) Current distributions for different leg separations. (c) Resistance and inductance variation as a function of S.

Using the electromagnetic field simulator SONNET, $|Z_T|$ is computed at three frequencies at and around 60 GHz and the results are used to determine the equivalent values of L_P, C_P, and R_P.[3]

For a given length, the folded microstrip of Fig. 2(a) provides two parameters that affect the performance: the linewidth W and the spacing between the legs S. Fig. 3(a) and (b) plots the tank parameters as W varies from 3 μm to 12 μm while the length of each leg is 155 μm and $S = 10$ μm. As expected, L_P falls, C_P rises, R_P increases to some extent, and $Q = R_P/(L_P\omega)$ improves. For amplification purposes, R_P must be maximized and L_P and C_P must be minimized so that the tank can absorb maximum transistor capacitance while resonating at 60 GHz. The plot in Fig. 3(c) quantifies these requirements, indicating diminishing returns as W exceeds 6 μm. Thus, a linewidth of 6 μm is used in this work.

The spacing between the two legs also plays a critical role in the design. For small S, the mutual magnetic coupling lowers the overall inductance, thus degrading the performance of the line. Fig. 4(a) depicts the distribution of the current as predicted by SONNET.[4] (Darker shades correspond to higher densities.) Based on these simulations, the current distribution in each leg (along the line AA$'$) can be plotted for different values of S [Fig. 4(b)]. As expected, greater values of S reduce the current density at the inner edges. From the circuit design point of view, we again consider the variation of R_P and L_P with S [Fig. 4(c)], noting that R_P reaches a relatively constant value for $S \approx 15$ μm (about twice the linewidth).[5] Thus, this value of S is chosen in this work.

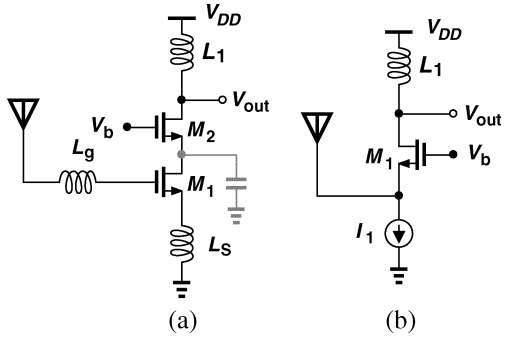

Fig. 5. (a) Cascode and (b) common-gate LNA topologies.

V. Building Blocks

A. LNA Design

Fig. 5 shows two candidates for the LNA design. At frequencies well below the f_T of the transistors, the cascode topology of Fig. 5(a) provides a low noise figure, good input matching, and a high reverse isolation. At 60 GHz, on the other hand, the pole at the drain of M_1 (typically on the order of $f_T/2$) shunts a considerable portion of the RF current to ground, thereby lowering the gain and raising the noise contributed by M_2. Furthermore, the small degeneration and gate series inductances (50–100 pH) required for input matching make the circuit very sensitive to package parasitics.

[3]Note that the self-resonance frequency of the structure is well above 60 GHz.

[4]The distributions are not exactly symmetric because one port of the folded microstrip is grounded.

[5]The Q varies only slightly here, from 10.3 to 12.2.

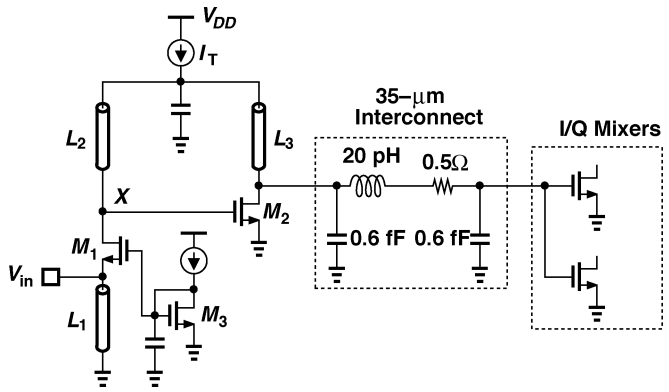

Fig. 6. LNA circuit diagram.

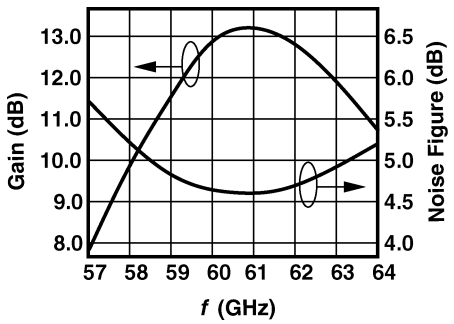

Fig. 7. Simulated LNA characteristics.

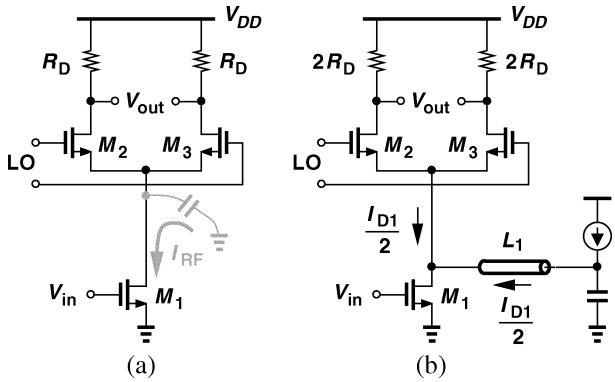

Fig. 8. (a) Conventional and (b) proposed mixer topologies.

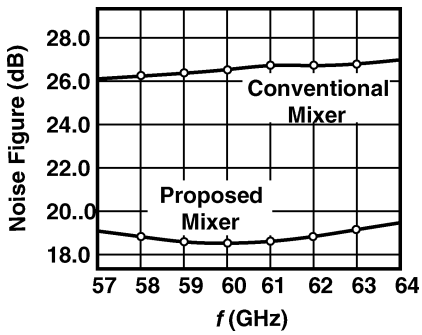

Fig. 9. Simulated noise figure for two mixer topologies.

The above observations suggest that the LNA must contain a single transistor before voltage amplification occurs, naturally pointing to the common-gate (CG) stage of Fig. 5(b). However, the required 50-Ω input resistance translates to a large transistor width (20 μm) and hence about 35 fF of input capacitance, degrading both the input match and the noise figure. That is, the capacitance seen at the source node must be cancelled by means of resonance. Similarly, the output node must also resonate so as to cancel the capacitance seen at the drain and introduced by the next stage. Moreover, the noise contributed by I_1 raises the noise figure considerably.

Fig. 6 shows the LNA implementation, where L_1 resonates with $C_{GS1} + C_{SB1}$ and the pad capacitance, and L_2 with the total capacitance at node X. Transistor M_2 provides additional gain and drive capability for the subsequent quadrature mixers. The three inductors are realized as the folded microstrip depicted in Fig. 2(a). With an equivalent parallel resistance of about 700 Ω, L_1 contributes negligible noise.

It is desirable to avoid AC coupling between the two stages of the LNA and between the LNA and the mixers. Metal-sandwich capacitors suffer from large bottom-plate parasitics, and lateral fringe structures may exhibit resonances close to the band of interest. A biasing scheme is introduced here that obviates the need for coupling capacitors. In the circuit of Fig. 6, transistor M_2 serves as a diode-connected device, carrying a current equal to $I_T - I_{D1}$. Thus, if the DC drops across L_2 and L_3 are negligible, M_2 forms a current mirror along with the common-source devices in the next stage, defining the bias current of the mixers.

Due to the physical dimensions of the folded microstrips in the layout, the LNA output must travel 35 μm before reaching the mixers. This interconnect is modeled by the simple network in the dashed box shown in Fig. 6. Fig. 7 plots the simulated voltage gain and noise figure of the LNA across the unlicensed band. The tradeoff between the maximum gain and the bandwidth suggests that varactor tuning of the LNA may be necessary. The circuit draws a supply current of 4 mA.

B. Mixer

Fig. 8 shows the conventional and proposed mixer topologies. According to simulations, the circuit of Fig. 8(a) exhibits a noise figure of 26 dB and a conversion gain of 0 dB. Several mechanisms account for this poor performance. First, the total capacitance at the drain of M_1 gives rise to a pole on the order of $f_T/2$. Second, since M_2 and M_3 must carry the entire bias current of M_1, they switch quite gradually, inject noise to the output, and "waste" part of the RF current as a common-mode component. Third, the limited supply voltage allows only a small voltage drop across the load resistors and hence a low conversion gain.

To alleviate these issues, we introduce the topology depicted in Fig. 8(b), where inductor L_1 (a folded microstrip) resonates with the total capacitance seen at the drain of M_1 and also carries about half of the drain current of M_1. Now, most of the RF current is commutated by M_2 and M_3 because the equivalent parallel resistance of L_1 is much greater than the average resistance seen looking into the sources of the switching pair. (For the same reason, the thermal noise contributed by L_1 is negligible.) Moreover, carrying a smaller current, M_2 and M_3 switch more abruptly. Finally, the load resistors can be doubled. As a result, the noise figure falls to about 18 dB and the conversion gain rises to 12 dB. The mixer core draws 0.9 mA. Fig. 9 plots the noise figure of the two topologies across the unlicensed band. In both cases, $(W/L)_1 = 4/0.13$ and $(W/L)_2 = (W/L)_3 = 10/0.13$.

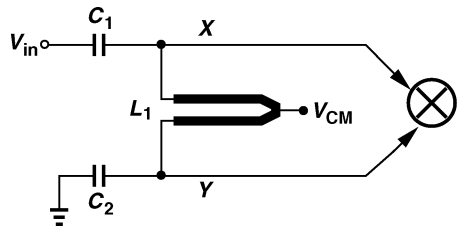

Fig. 10. Balun realization.

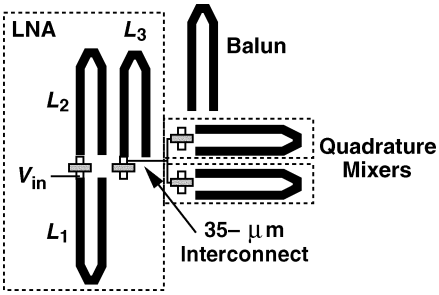

Fig. 11. Receiver floor plan.

C. Balun

As mentioned in Section III, a balun is included on the chip to facilitate testing. Shown in Fig. 10, the circuit consists of two equal coupling capacitors C_1 and C_2 (realized as metal sandwiches) and an inductor L_1 (implemented as a folded microstrip). For $C_1 = C_2 = C$,

$$\frac{V_X}{V_Y} = 1 - L_1 C\omega^2 \tag{1}$$

$$= -1 \text{ at } \omega_0 = \frac{1}{\sqrt{L_1 \frac{C}{2}}}. \tag{2}$$

The balance between X and Y is degraded to some extent by the input capacitance of the mixer and the parasitics of L_1.

D. Output Buffer

The output buffer consists of a simple differential pair followed by open-drain common-source devices that can drive 50-Ω instrumentation. The targeted voltage gain is about 12 dB to ensure the receiver output noise overwhelms the noise floor of spectrum analyzers and noise figure meters. As such, the buffer exhibits a (simulated) 1-dB compression point of about 100 mV_{rms} (equivalent to −7 dBm in a 50-Ω system) and tends to limit the linearity of the receiver.

VI. Experimental Results

The receiver front-end has been designed and fabricated in digital 0.13-μm CMOS technology. Fig. 11 shows the floor plan. Note that the folded microstrips allow placement of the active devices in close proximity, with only one long interconnect (35 μm). Also, the wide ground planes under the microstrips serve as a low-impedance return path throughout the chip.

Fig. 12 depicts the die, whose active area measures 400 μm × 300 μm. The circuit has been tested on a Cascade probe station while operating with a 1.2-V supply. Since 60-GHz cables and probes suffer from a high loss, an on-chip pad frame is used to measure the loss of two back-to-back sets of cables and probes. Table I summarizes the measured performance of the receiver.

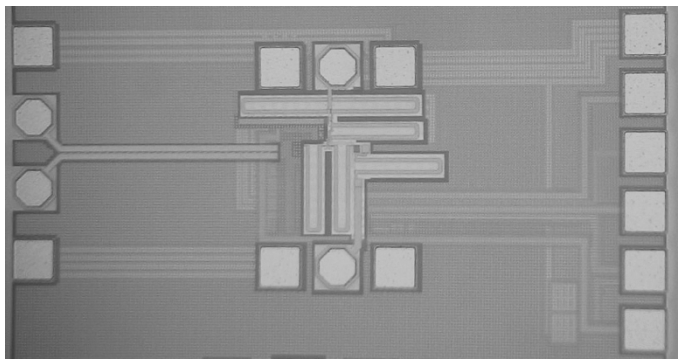

Fig. 12. Die photograph.

TABLE I
Measured Performance of Receiver

Voltage Gain	28 dB
Noise Figure	12.5 dB
1–dB Compression Point	–22.5 dBm
Power Dissipation	9 mW
Supply Voltage	1.2 V
Active Area	300 um x 400 um
Technology	0.13–um CMOS

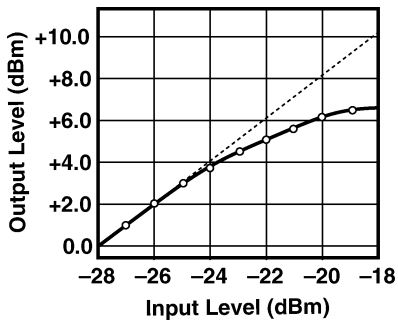

Fig. 13. Input/output characteristic of the front-end.

The gain is measured as follows. The signal level provided by the 60-GHz generator is measured by means of an accurate power meter and subsequently applied to the circuit through a variable attenuator. The downconverted signal is monitored on a spectrum analyzer, and the measured loss of the input cable and probe is taken into account. Fig. 13 plots the input/output characteristic.

The noise figure is measured using two approaches.[6] In the first approach, a 60-GHz signal with a level of −35 dBm (measured accurately by a power meter and a variable attenuator) is applied to the receiver. The input SNR in 1 Hz is thus equal to 174 dBm − 35 dBm = 139 dBm. The downconverted signal at an intermediate frequency of 100 MHz is then displayed on a spectrum analyzer and the output SNR in 1 Hz is measured. The loss of the input cable and probe is then subtracted from the difference between these SNRs (all in dB) to obtain the noise figure.

[6]No shield room was available for these measurements.

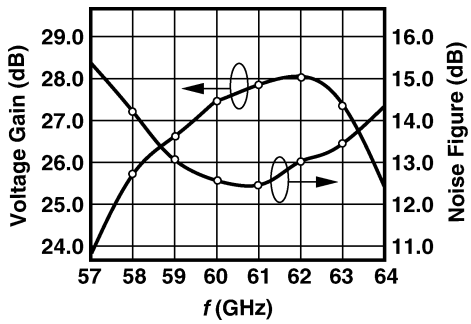

Fig. 14. Voltage gain and noise figure.

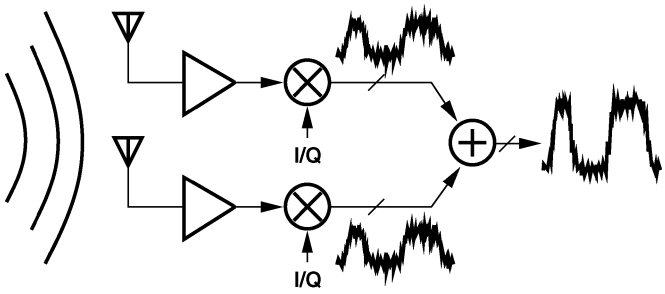

Fig. 15. Use of two antennas and receivers to reduce noise figure.

In the second approach, a 60-GHz noise generator and a standard noise figure meter are used. The two methods yield nearly the same results. Fig. 14 plots the voltage gain and noise figure across the unlicensed band.

The voltage gain and the noise figure are, respectively, 8 dB lower and 4 dB higher than simulated values. The source of these discrepancies is unknown at this point but LO imbalance due to the balun and noise picked up by the probe station are possible causes.

VII. Conclusion

CMOS technology is poised to enter the millimeter-wave regime and supplant many III-V circuits. This paper has investigated the properties of folded microstrips for amplification at 60 GHz and introduced new CMOS LNA and mixer topologies that exploit resonant devices to operate at high frequencies. A receiver front-end employing these concepts achieves a noise figure of 12.5 dB and a gain of 28 dB while consuming 9 mW.

The remarkably low power dissipation and small area of the receiver offer interesting possibilities for higher performance. For example, suppose two antennas and two receivers are integrated as shown in Fig. 15. Even without sophisticated antenna diversity and beam forming techniques, the baseband voltages of the two receivers can be added to improve the signal-to-noise ratio by 3 dB with a total power dissipation of less than 20 mW. Note that phase coherence at the two antennas (at 60 GHz) is not critical; only the baseband data streams must have a reasonable phase alignment.

Acknowledgment

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References

[1] M. Banu, "MOS oscillators with multi-decade tuning range and gigahertz maximum speed," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1386–1393, Dec. 1988.

[2] B. Kleveland *et al.*, "Monolithic CMOS distributed amplifier and oscillator," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 1999, pp. 70–71.

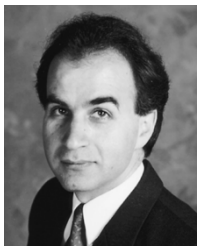
[3] L. M. Franca-Neto, R. E. Bishop, and B. A. Bloechel, "64-GHz and 100-GHz VCO's in 90-nm CMOS using optimum pumping method," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2004, pp. 444–445.

[4] F. Ellinger, " 26-42 GHz SOI CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 522–528, Mar. 2004.

[5] C. H. Doan *et al.*, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.

[6] *IEEE Std 802.162004, IEEE Standard for Local and Metropolitan Area Networks, Part 16: Air Interface for Fixed Broadband Wireless Access Systems*, 2004.

[7] H. Li and H. M. Rein, "Millimeter-wave VCOs with wide tuning range and low phase noise, fully integrated in a SiGe bipolar production technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 184–191, Feb. 2003.



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Prof. Razavi served on the Technical Program Committees of the International Solid-State Circuits Conference (ISSCC) from 1993 to 2002 and VLSI Circuits Symposium from 1998 to 2002. He has also served as Guest Editor and Associate Editor of the IEEE Journal of Solid-State Circuits, IEEE Transactions on Circuits and Systems, and the *International Journal of High Speed Electronics*. He received the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the Best Paper Award at the 1994 European Solid-State Circuits Conference, the Best Panel Award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, and the Best Paper Award at the IEEE Custom Integrated Circuits Conference in 1998. He was the co-recipient of both the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence at the 2001 ISSCC. He was also recognized as one of the top 10 authors in the 50-year history of ISSCC. He is an IEEE Distinguished Lecturer and a Fellow of IEEE.