CHAPTER 10

Operational Amplifier Circuits

10.1 INTRODUCTION

In this chapter we present a number of linear and nonlinear op amp circuits to show the wide range of possible applications. A brief explanation is given for each circuit along with pertinent waveforms, impedances, and some specific applications.

10.2 THE INVERTING AMPLIFIER

Perhaps the simplest of all op amp circuits is the inverting amplifier shown in Fig. 10.1. As we have seen in Chapter 9, the exact voltage gain expression is

$$A_v = \frac{-\dfrac{R_2}{R_1}}{1 + \dfrac{R_1 + R_2}{A_o R_1}} \tag{10.1}$$

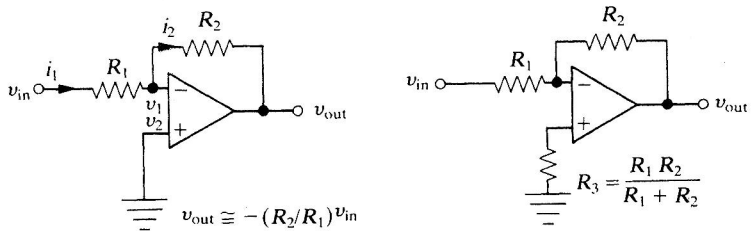
If $A_o R_1 \gg (R_1 + R_2)$, which is almost always the case, we have the simple gain expression

$$A_v \cong -\frac{R_2}{R_1} \tag{10.2}$$

(10.2) can also be derived immediately by using the two op amp rules of Chapter 9, which we repeat here for convenience:

I. Op amp current rule (OACR): The current flowing into (or out of) each op amp terminal is zero.
II. Op amp voltage rule (OAVR): The voltage difference between the inverting and the noninverting terminals is zero.

As a review, we repeat the voltage gain derivation, using the two rules.



(a) *basic circuit* (b) *compensated for bias current*

FIGURE 10.1 The inverting amplifier.

The OACR implies $i_1 = i_2$, and the OAVR implies $v_2 = v_1$. Thus, using Ohm's law to evaluate i_1 and i_2, we have $v_{in}/R_1 = -v_{out}/R_2$, or $v_{out}/v_{in} = -R_2/R_1$.

The input resistance is simply equal to R_1, because by the OAVR the voltage at the inverting input must be zero. The inverting input is termed a *virtual ground*. Notice that this is true regardless of the value of R_1 or R_2—that is, regardless of the circuit gain.

The output resistance of the amplifier circuit of Fig. 10.1 is reduced to below that of the bare (no feedback) op amp by the negative feedback and is given by

$$R_{out} = \frac{r_{out}}{1 + \dfrac{R_1 A_o}{R_1 + R_2}} \cong \frac{1 + \dfrac{R_2}{R_1}}{A_o} r_{out} \cong \frac{A_v}{A_o} r_{out} \tag{10.3}$$

where r_{out} is the output resistance of the bare op amp. Typical values of the output resistance R_{out} are extremely low—a few ohms or less.

The circuit bandwidth (BW) (see 9.8.1) depends on the gain with feedback, A_v: the smaller the gain the larger the bandwidth. For most op amps the open-loop op amp voltage gain decreases as $1/f$ (20 dB/decade or 6 dB/octave) for $f > f_B$; f_B is the break frequency where the op amp open-loop gain A_o is 3 dB down from its dc value. f_B is usually 100 Hz or less. Thus,

$$\text{BW} = f_B\left(\frac{A_o}{A_v}\right) \tag{10.4}$$

This is simply another way of writing the constant gain bandwidth product: $(\text{BW})A_v = f_B A_o$. For example, if the open-loop gain break frequency is $f_B = 500$ Hz, and the open-loop gain is 10^5, then for a gain of 20 the bandwidth would be $\text{BW} = (500\ \text{Hz})(10^5)/20 = 2.5 \times 10^6$ Hz.

The input resistance for the noninverting circuit of Fig. 10.2 is much larger than for the inverting circuit of Fig. 10.1. From either direct analysis or the feedback theory of Chapter 8, the input resistance of the amplifier is

$$R_{in} = (1 + A_o B)R_{ino} \cong \frac{A_o}{A_v} R_{ino} \tag{10.9}$$

where R_{ino} is the input resistance of the bare op amp (usually very large) and can be estimated from the bias current I_B given in the op amp spec sheet. For example, if the bias current is 1 nA, then $R_{ino} \approx 1\text{ V}/I_B \cong 1\text{ V}/10^{-9}\text{ A} = 10^9\ \Omega$. In most cases the input resistance of the noninverting amplifier is so large it can be considered infinite for all practical purposes. Thus, it is common practice to wire in a resistance $R' \cong 100\text{ k}\Omega$ from the noninverting input to ground to stabilize the input impedance. (Some dc resistance R' to ground is absolutely essential if the input is ac coupled.)

The output resistance R_{out} of the noninverting amplifier circuit of Fig. 10.2 is

$$R_{out} = \frac{R_o}{1 + A_o B} \cong R_o \frac{A_v}{A_o} \tag{10.10}$$

where R_o is the output resistance of the base op amp with no feedback. Typical values of R_{out} are extremely low—several ohms or less.

The bandwidth is the same as for the inverting amplifier:

$$\text{BW} = f_B\left(\frac{A_o}{A_v}\right) \tag{10.11}$$

where f_B is the frequency where the op amp open-loop gain is 3 dB less than the dc gain, A_o is the dc open-loop gain, and $A_v = 1 + R_2/R_1$ is the circuit gain with feedback.

The dc output with zero input is

$$v_{oo} = \pm V_{io}\left(1 + \frac{R_2}{R_1}\right) + I_B R_2 \tag{10.12}$$

With the addition of $R_3 = R_1 R_2/(R_1 + R_2)$ in series with the noninverting input, as shown in Fig. 10.2(b), the dc output with zero signal input is

$$v_{oo} = \pm V_{io}\left(1 + \frac{R_2}{R_1}\right) \pm I_{io} R_2 \tag{10.13}$$

which is the *same* as for the inverting amplifier.

A special case of the noninverting amplifier is the voltage follower shown in Fig. 10.2(c). It is the noninverting amplifier with $R_2 = 0$, and $R_1 \to \infty$; in other words, all the output voltage is fed back. The voltage follower thus has a voltage gain of 1, but a very high input resistance and a very low output resistance, and a large bandwidth. Thus, it is useful as a buffer amplifier when it is desirable to isolate two parts of a system. It is almost an ideal one-way device because of its high input and low output resistances—changes at the output will have almost no effect on its input, and it will draw almost no current from its input. In other words, it acts as an impedance transformer; it allows us to couple a signal from a source with a high output resistance (such as a glass pH electrode, a wick electrode in neurophysiology, or a photomultiplier tube) to a lower impedance circuit.

Actual measurements of these parameters for some popular op amps are shown in Table 10.2 for $R_1 = 1\text{ k}\Omega$, $R_2 = 100\text{ k}\Omega$ in Fig. 10.2(a).

TABLE 10.2. Noninverting Amplifier Parameters

Op Amp	A_v	R_{out} (Ω)†	*BW (kHz)*	*GBW (MHz)*
741	94	2	10	0.94
318*	92	140	200	18
071	96	1	34	3.3

*5 pF in parallel with $R_2 = 100\text{ k}\Omega$.
†at 1 kHz.

10.4 THE DIFFERENTIAL AMPLIFIER

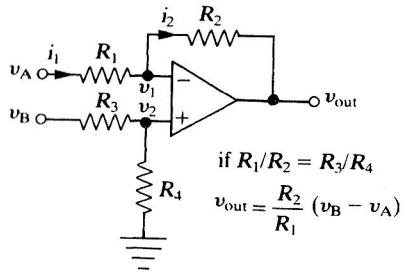
A difference or differential amplifier is one whose output is proportional to the difference between two input voltages $v_{out} = A_v(v_B - v_A)$. The amplifier is shown in Fig. 10.3(a). Such an amplifier is useful when both signals contain large (and equal) amounts of noise, such as 60-Hz pickup. This is often the case when the input signals come fron transducers that have a high impedance to ground (biological wick electrodes, for example). Another useful application is when the dc level of the two inputs is high (several volts) and when the signal change is small (millivolts). This is the case for strain gauges.

Applying the OACR and the KCL to the junction at the inverting input, we have

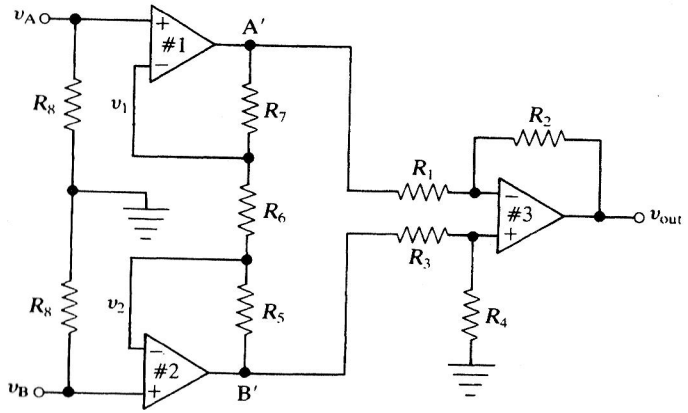
$$i_1 = i_2 \qquad \frac{v_A - v_1}{R_1} = \frac{v_1 - v_{out}}{R_2} \tag{1}$$

The OAVR implies $v_1 = v_2$, but v_2 is given by

$$v_2 = \frac{R_4}{R_3 + R_4} v_B = v_1 \tag{2}$$



(a) *basic circuit*



(b) *instrumentation amplifier*

FIGURE 10.3 The difference amplifier.

Eliminating v_1 between (1) and (2), we get

$$v_{out} = \frac{R_2}{R_1}\frac{1 + \dfrac{R_1}{R_2}}{1 + \dfrac{R_3}{R_4}}(v_B - v_A)$$

If we choose the resistances such that $R_1/R_2 = R_3/R_4$, then the output is given by

$$v_{out} = \frac{R_2}{R_1}(v_B - v_A) \qquad \textbf{(10.14)}$$

which indicates that the output is proportional to the difference between the two input voltages v_B and v_A.

The resistances must be chosen carefully to satisfy $R_1/R_2 = R_3/R_4$. Resistances of 1% or better tolerance are generally required to get a high CMRR. If (10.14) holds exactly, the CMRR = ∞; that is, the gain for $v_A = v_B$ is zero. Also, notice that the input impedances for v_A and v_B are different, being much higher for v_B. This can be a very serious source of noise pickup.

The usual instrumentation amplifier consists of three op amps and is shown in Fig. 10.3(b). Op amp #3 and R_1, R_2, R_3, and R_4 comprise the standard basic circuit of Fig. 10.3(a). Thus, the output is given by

$$v_{out} = \frac{R_2}{R_1}(v_{B'} - v_{A'}) \qquad \textbf{(1)}$$

if $R_1/R_2 = R_3/R_4$.

The input impedance for both v_A and v_B is R_8 because both inputs go directly to the high impedance noninverting input terminals. From the OAVR we have

$$v_1 = v_A \quad \text{and} \quad v_2 = v_B$$

Thus, for a common mode input ($v_A = v_B$) there is zero voltage drop across R_6, and therefore no current flows through the R_5, R_6, R_7 resistor chain. Thus, $v_{A'} = v_{B'}$, and there is zero differential input to op amp #3, and v_{out} is zero. But for a differential input ($v_A \neq v_B$) the same current must flow through the R_5, R_6, R_7 chain because zero current flows into the inverting input terminals of op amps #1 and #2. Thus,

$$\frac{v_{A'} - v_1}{R_7} = \frac{v_1 - v_2}{R_6} = \frac{v_2 - v_{B'}}{R_5} = \frac{v_{A'} - v_{B'}}{R_5 + R_6 + R_7} \qquad \textbf{(2)}$$

Solving for $v_{B'} - v_{A'}$, we obtain

$$v_{B'} - v_{A'} = -\frac{R_5 + R_6 + R_7}{R_6}(v_B - v_A)$$

It is common practice to choose $R_5 = R_7 = R$, so the gain expression becomes

$$v_{out} = -\frac{R_2}{R_1}\left(1 + \frac{2R}{R_6}\right)(v_B - v_A) \qquad \textbf{(10.15)}$$

The overall differential gain can be set by adjusting R_6.

Many different commercial instrumentation amplifiers are available at prices from less than a dollar to hundreds of dollars. One such (expensive) instrumentation FET amplifier is the 4253, which is especially

TABLE 10.3. Selected Instrumentation Amplifier Specifications

Parameter	*4253*	*LF152*	*AD624A*
Circuit gain	1–10,000	1 to 1000	1 to 1000
Output impedance ($A_v = 1$)	0.1 Ω max @ dc 1.0 Ω max @ 3 kHz	1.2 Ω	
Output swing	±10 V @ ±5 mA	±9 V	±10 V
Output capacitive load	max 0.01 μF		
Input impedance	10^{13} Ω‖3 pF diff. or cm	2×10^{12} Ω‖2.5 pF diff. 2×10^{12} Ω‖5.0 pF cm	10^9 Ω
Input swing	±36 V max	±12 V (*must* not exceed $-V_{CC}$)	±10 V max
CMRR	76 dB dc to 60 Hz $A = 1, 10$ 114 dB dc to 100 Hz $A = 1000$ 108 dB dc to 500 Hz $A = 1000$	85 dB $A = 1$ 105 dB $A = 10$ 125 dB $A = 100$ 125 dB $A = 1000$	70 dB $A = 1$ 100 dB $A = 10$ 110 dB $A = 1000$
Input offset voltage	±1 mV RTI max ± 4 μV/°C ±15 mV RTO max ± 100 μV/°C ±3 μV/% power supply drift ±5 μV/day shift	8 mV 10 μV/°C ±100 μV/V power supply	200 μV 2 μV/°C
Input noise voltage	1.6 to 160 Hz 0.3 μV_{rms} RTI 1.6 to 160 Hz 30 μV_{rms} RTO	10 Hz to 10 kHz $8 + 450/A$ μV_{rms}	0.2 μV 0.1 to 10 Hz $A = 1000$
Input bias current	−10 pA max @ 25°C(×2/10°C) −55 pA @ 50°C 0.05 pA/V cm input 0.05 pA/V signal input 0.02 pA/% power supply drift	3 pA @ 25°C (0.5 pA offset current)	±50 nA ±50 pA/°C
Slew rate		1 V/μS	5 V/μs
Input current noise	1.6 to 160 Hz 1 pA_{rms}	10 Hz to 10 kHz 0.01 pA_{rms}	
Power supply	±15 V @ ±21 mA_{max} (full load)	±22 V 0.7 mA	±5 to 18 V @ 3.5 mA

suited for amplifying small differential signals in the presence of large common mode voltages. It has a very high input impedance, low drift with time and temperature, low input noise, low bias current, adjustable gain with one external resistor, and output short circuit protection. The 4253 specifications are listed in Table 10.3. A less expensive instrumentation amplifier is the AD624A.

10.5 THE OP AMP POWER BOOSTER

Most inexpensive op amps can put out a maximum current of approximately 10 to 20 mA before the output waveform is seriously distorted. The circuit shown in Fig. 10.4(a) will boost the output current (and power) to the limits of the transistor, which can be chosen to be a high-power transistor. The circuit of Fig. 10.4(a) has one disadvantage, however; its output voltage is always positive (or negative if a pnp transistor and negative supply are used). Thus, this circuit can only "source" current; it cannot "sink" current. Notice that the output transistor is *inside* the feedback loop and is acting essentially as an emitter follower. From basic negative feedback theory $B = R_1/(R_1 + R_2)$, and the overall voltage gain of the op amp and transistor of Fig. 10.4(a) must be

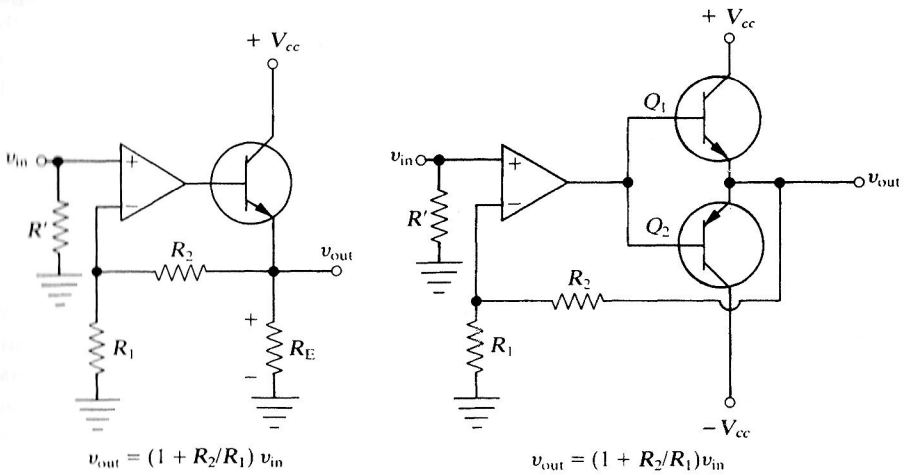
$$A = \frac{1}{B} = 1 + \frac{R_2}{R_1} \tag{10.16}$$

If both positive and negative output voltage swings are desired, the bottom of R_E can be tied to a negative supply voltage or the push-pull circuit of Fig. 10.4(b) can be used. If the op amp output swings positive, then the npn transistor Q_1 is turned on and Q_2 is turned off; hence the output voltage goes positive. If the op amp swings negative, then the pnp transistor Q_2 is turned on and Q_1 is turned off; hence the output goes negative. You might recall that the turn-on voltage for any silicon transistor is approximately 0.5 V and thus might be tempted to conclude that the op amp output would have to be at least ±0.5 V to get a nonzero output and that therefore the output will be seriously distorted. This is not the case because the transistors are *inside* the feedback loop. The OAVR states that the voltage at the noninverting input terminal (v_{in}) must equal the voltage at the inverting terminal, which is $R_1/(R_1 + R_2)$ times the *output* voltage:

$$v_{in} = \frac{R_1}{R_1 + R_2} v_{out}$$

Thus, the overall voltage gain of the op amp plus transistors is

$$A = \frac{v_{out}}{v_{in}} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1} \tag{10.17}$$



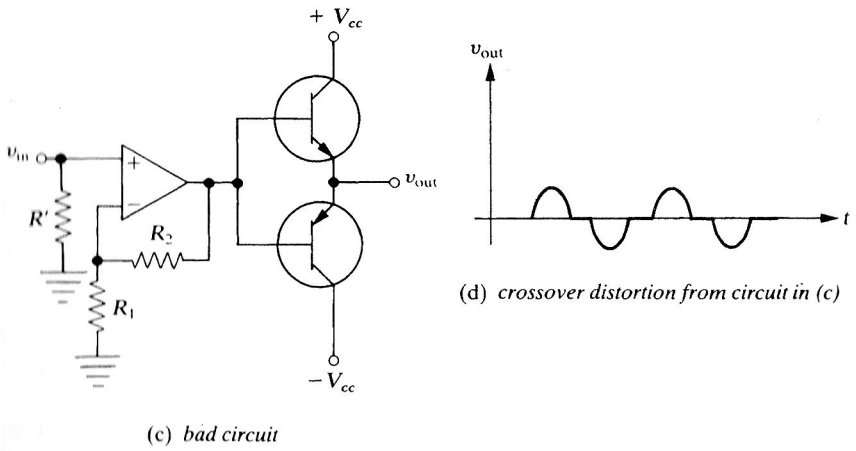


FIGURE 10.4 Power booster.

Push-pull transistors are available on a single chip that will supply up to several hundred mA of output current. Examples are the MC1438 and the LH0063.

It is instructive to investigate what would happen if the output transistors were outside the feedback loop, as shown in Fig. 10.4(c). In this case the output of the op amp would have to be greater than approximately 0.5 V (either + or −) to turn on one of the output transistors. Thus, the output would "miss" the first 0.5 V of signal and would look like Fig. 10.4(d) for a pure sinusoidal input. Such distortion is called *crossover* distortion, because it occurs as the input signal crosses or changes polarity.

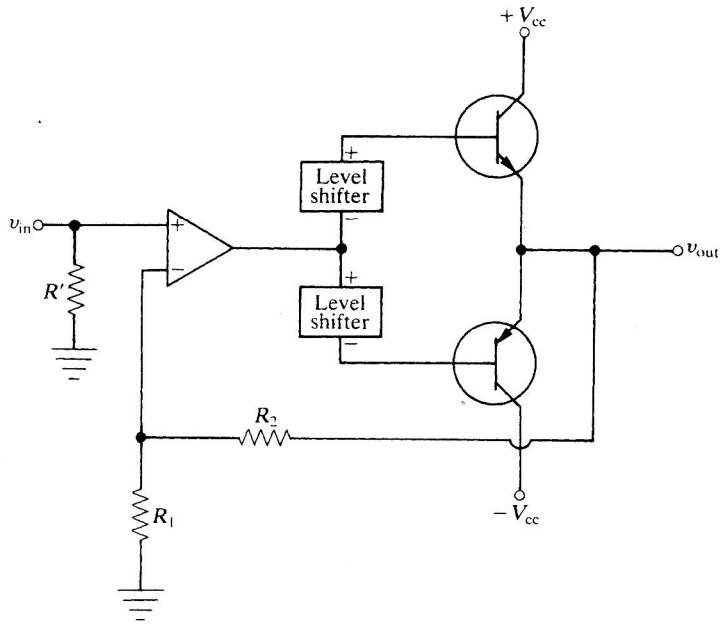


FIGURE 10.5 Push-pull power booster with level shifter.

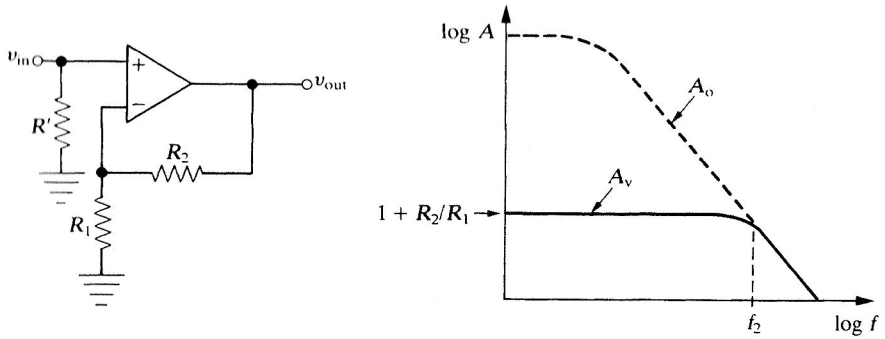
If minimum distortion is required, the crossover distortion can be decreased even more by adding level-shifter circuits (see 9.5.1), as shown in Fig. 10.5. Both the npn and the pnp transistors are biased slightly on by the level shifter even with zero signal from the output of the op amp. The price paid is the higher power dissipation in the transistors with zero input signal.

10.6 COMPENSATION OR EQUALIZATION AMPLIFIERS

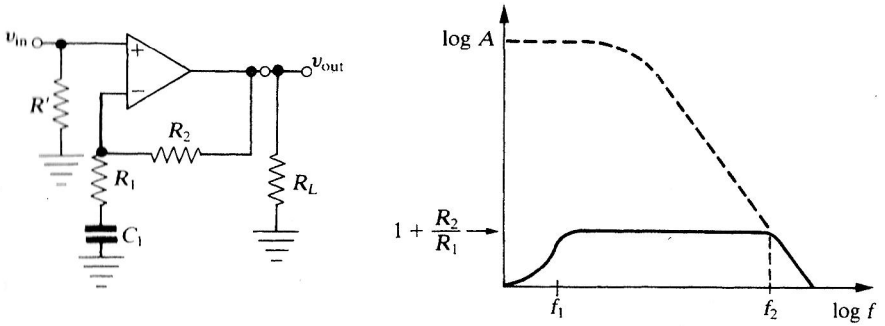
The conventional noninverting op amp of Fig. 10.6(a) has a flat frequency response out to f_2; it will amplify signals from dc up to f_2 with a gain of $1 + R_2/R_1$. The gain at f_2 will be 3 dB less than the dc gain.

To avoid having the dc output level depend on the slowly drifting (due to aging or temperature changes) op amp voltage offset and bias current, it is often desirable to decrease the amplifier gain at dc and low frequencies. A capacitance C_1 in series with R_1 will accomplish this, as shown in Fig. 10.6(b). There must be some dc path from the inverting output to ground through v_{out}, shown in Fig. 10.6(b) as R_L. The voltage gain will be

$$A = 1 + \frac{R_2}{Z_1}$$

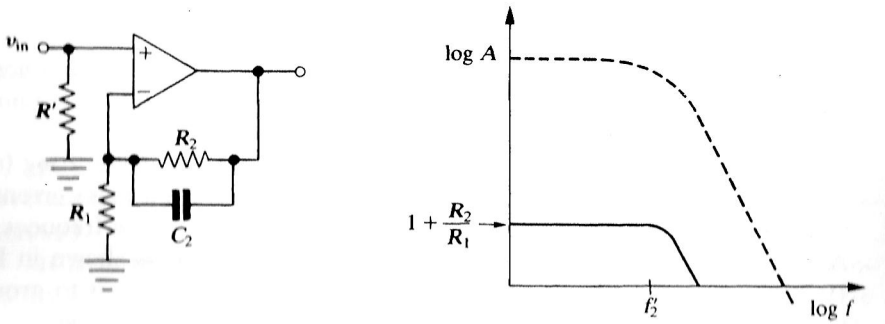


(a) *dc coupled*



$$f_1 = \frac{1}{2\pi R_1 C_1} \text{ or } \omega_1 = \frac{1}{R_1 C_1}$$

(b) *ac coupled to reduce dc gain*



$$f_2' = \frac{1}{2\pi R_2 C_2} \text{ or } \omega_2' = \frac{1}{R_2 C_2}$$

(c) *reduced high-frequency gain*

FIGURE 10.6 Equalization amplifiers.

where Z_1 is the series impedance of R_1 and C_1: $Z_1 = R_1 + 1/j\omega C_1$. Thus, the amplifier gain is

$$A = 1 + \frac{R_2}{R_1 + \dfrac{1}{j\omega C_1}} = 1 + \frac{j\omega R_2 C_1}{1 + j\omega R_1 C_1}$$

If we let $\omega_1 = 1/R_1 C_1$, then we can write the gain as

$$A = 1 + \frac{\dfrac{j\omega R_2}{\omega_1 R_1}}{1 + \dfrac{j\omega}{\omega_1}} \tag{10.18}$$

If $\omega \gg \omega_1$, then $A \to 1 + R_2/R_1$, which is the midfrequency gain. If $\omega \ll \omega_1$, then $A \cong 1 + j(\omega/\omega_1)R_2/R_1$, which decreases (to 1) with decreasing frequency. At $\omega = \omega_1$, $A \cong 1/\sqrt{2}(R_2/R_1)$ if $R_2/R_1 \gg 1$, that is, A is 3 dB less than the midfrequency gain. The gain-versus-frequency curve is shown in Fig. 10.6(b).

Similarly, to reduce the gain at high frequencies (but less than f_2), we can add a capacitance C_2 in parallel with R_2, as shown in Fig. 10.6(c). The voltage gain will then be

$$A = 1 + \frac{Z_2}{R_1}$$

where Z_2 is the parallel impedance of R_2 and C_2:

$$Z_2 = \frac{R_2\left(\dfrac{1}{j\omega C_2}\right)}{R_2 + \dfrac{1}{j\omega C_2}} = \frac{R_2}{1 + j\omega R_2 C_2}$$

Thus,

$$A = 1 + \frac{\dfrac{R_2}{R_1}}{1 + j\omega R_2 C_2}$$

If we let $\omega_2 = 1/R_2 C_2$, then the gain can be written as

$$A = 1 + \frac{\dfrac{R_2}{R_1}}{1 + \dfrac{j\omega}{\omega_2}} \tag{10.19}$$

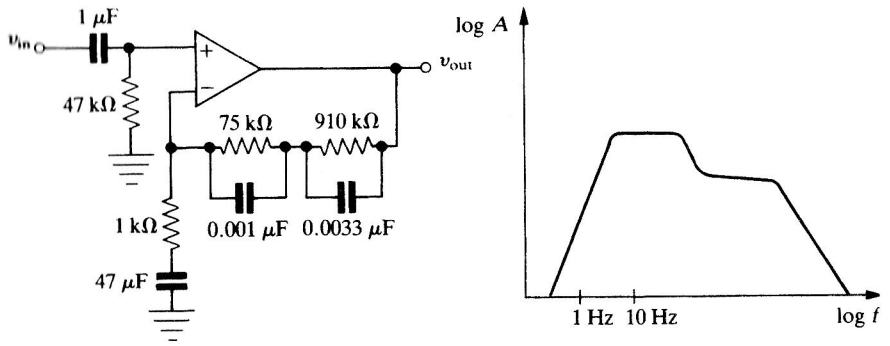


FIGURE 10.7 RIAA phonograph compensation amplifier.

Thus if $\omega \ll \omega_2'$, $A \to 1 + R_2/R_1$, which is the midband gain; if $\omega \gg \omega_2'$, $A \to 1 + R_2\omega_2/j\omega R_1$, which decreases (to 1) with increasing frequency. At $\omega = \omega_2'$, $A \cong 1/\sqrt{2}(R_2/R_1)$ if $R_2/R_1 \gg 1$, that is, A is 3 dB less than the midfrequency gain. The gain-versus-frequency curve is shown in Fig. 10.6(c).

The popular RIAA compensation curve for LP phonograph records can be created with three capacitors, as shown in Fig. 10.7. The 1-μF, 47-kΩ high-pass RC filter at the input has a break frequency of 3.4 Hz.

10.7 THE SUMMING AMPLIFIER

An op amp can easily be hooked up to act as an adder; that is, the output voltage will be the sum of a number of independent input voltages (with each input multiplied by its own gain if desired). The circuit is shown in Fig. 10.8; it uses the fact that for the inverting configuration the inverting input is a virtual ground, which means that the various inputs are electrically isolated from each other. No input should affect any other input.

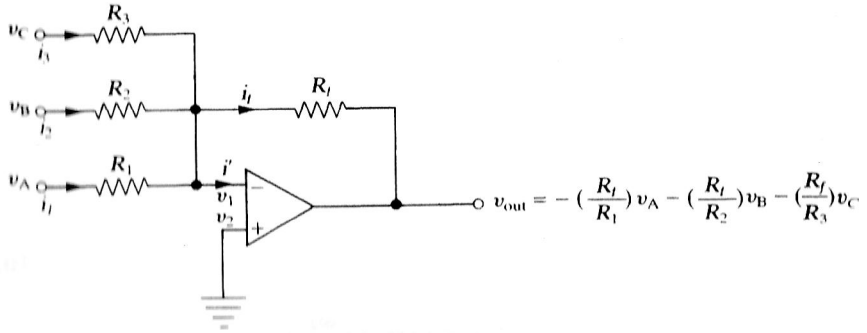


FIGURE 10.8 The summing amplifier.

The output voltage expression can be obtained easily by writing the KCL at the inverting input:

$$i_1 + i_2 + i_3 = i_f + i'$$

Neglecting i' from the OACR and using Ohm's law give

$$\frac{v_A - v_1}{R_1} + \frac{v_B - v_1}{R_2} + \frac{v_C - v_1}{R_3} = \frac{v_1 - v_{out}}{R_f}$$

But $v_1 = v_2 = 0$ from the OAVR, so the output is

$$v_{out} = -\left(\frac{R_f}{R_1}\right)v_A - \left(\frac{R_f}{R_2}\right)v_B - \left(\frac{R_f}{R_3}\right)v_C \qquad \textbf{(10.20)}$$

Thus we see that the output is a linear sum (with negative coefficients) of the inputs. If $R_1 = R_2 = R_3 = R_f$, then the output is $v_{out} = -v_A - v_B - v_C$. The output can easily be made positive by simply adding an inverting amplifier to the output.

This summing circuit can be made into a digital-to-analog converter very simply—v_A is the least significant bit, v_B the next more significant bit, and so on. We then choose the resistances so that $R_2 = R_1/2$, $R_3 = R_2/2$, and so on, so that v_B will be weighted twice as heavily in the output as v_A, and so forth. This will be explained at greater length in Chapter 15.

10.8 THE CURRENT-TO-VOLTAGE CONVERTER (THE TRANSCONDUCTANCE AMPLIFIER)

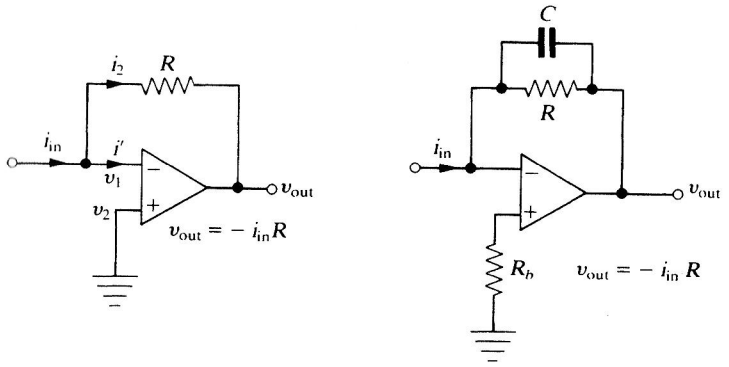
It is often desirable to convert a small input current to an output voltage for further processing. Examples of input current sources are a phototube, a photovoltaic cell, a photomultiplier tube, a photodiode, and a phototransistor. The op amp circuit of Fig. 10.9 does the trick; the output voltage equals the negative of the input current times the feedback resistance R. The KCL at the inverting input implies

$$i_{in} = i_2 + i'$$

The OACR implies $i' = 0$. But Ohm's law implies

$$i_2 = \frac{v_1 - v_{out}}{R}$$

But the OAVR implies $v_1 = v_2$, and $v_2 = 0$, so



(a) *basic circuit* (b) *reduced high-frequency gain from C, reduced output offset from R_b*

FIGURE 10.9 Current-to-voltage converter.

$$i_{in} = \frac{-v_{out}}{R}$$

or

$$v_{out} = -i_{in}R \qquad \textbf{(10.21)}$$

For example, if $R = 1\,\text{M}\Omega$, then a 1-μA input current will produce a 1-V output. We say the output will be 1 V/μA. If $R = 5\,\text{M}\Omega$, we would have 5 V/μA. The reader might well ask, Why not just run the current directly through the resistance R and avoid the expense of the op amp? After all, the output voltage will still be 1 V/μA for $R = 1\,\text{M}\Omega$. The answer is that the op amp provides *power* gain; in other words, the output impedance of the op amp is much less than R and thus can drive a wide variety of circuits. If the output were taken off R directly (without the op amp), there would be no power gain and the output resistance would be high. The op amp circuit also provides much better isolation between the input and output.

If only low-frequency or slow dc variations in the input current are of interest, it is desirable to connect a capacitance in parallel with R as shown in Fig. 10.9(b) to reduce the high-frequency gain so that high-frequency pickup and possible oscillations are prevented. The maximum frequency response of the circuit will then be approximately

$$2\pi f_{max} = \omega_{max} \cong \frac{1}{RC}$$

because the output voltage cannot change in a time shorter than the RC time constant.

A resistance R_b in series with the noninverting input might be necessary to decrease the dc output voltage due to the offset bias current of the op amp, as shown in Fig. 10.9(b). R_b can be adjusted to zero the output voltage at any fixed temperature, but temperature changes will always change the output dc voltage due to the temperature coefficient of the bias current.

10.9 THE VOLTAGE-TO-CURRENT CONVERTER

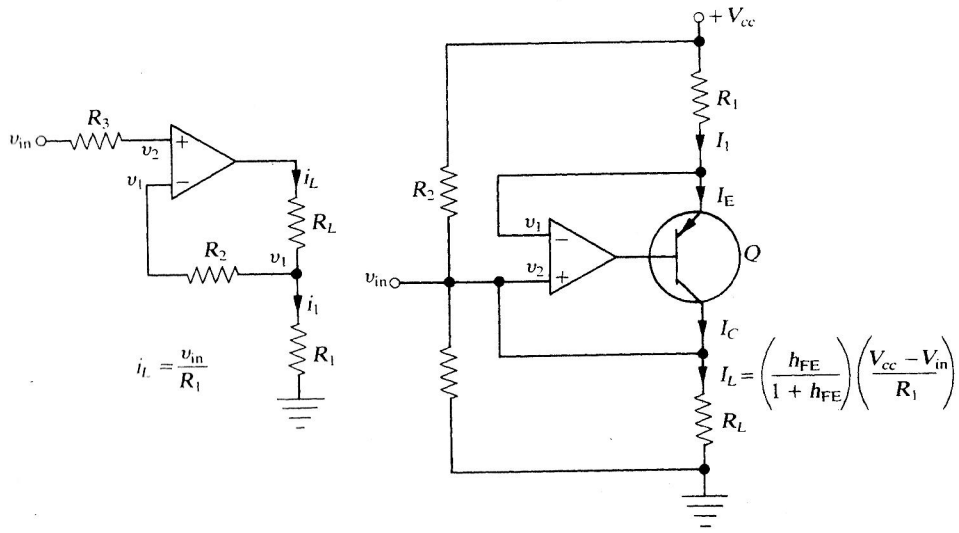
The circuit of Fig. 10.10(a) will supply a current through the "load" resistance R_L, which is independent of R_L; the current equals the input voltage divided by R_1.

Because the op amp inputs draw negligible current (OACR), there is no voltage drop across R_3 and the input voltage equals the voltage at the noninverting terminal: $v_{in} = v_2$. The OAVR implies $v_2 = v_1$, and there is no current through or voltage drop across R_2 from the OACR, so $v_1 = i_1R_1$. Thus

$$v_{in} = v_2 = v_1 = i_1R_1$$

But $i_1 = i_L$ because no current flows through R_2 into the inverting input. Thus

$$v_{in} = i_LR_1$$



(a) *"floating" load* (b) *one end of load grounded*

FIGURE 10.10 Voltage-to-current converter.

or the current through the load R_L is simply

$$i_L = \frac{v_{in}}{R_1} \tag{10.22}$$

Notice:

1. The load current can be changed by changing the input voltage.
2. No current (or power) is drawn from the v_{in} source.
3. The load current is independent of the load resistance R_L.
4. The maximum load current is the maximum current output of the op amp, which is typically 20 mA for an inexpensive general-purpose op amp.
5. Both ends of the load resistance are above ground.
6. R_2 and R_3 can be adjusted to minimize op amp bias current efforts on the output.

If one end of the load resistance must be grounded, the circuit of Fig. 10.10(b) can be used.

By the OACR, $I_1 = I_E$ and $I_C = I_L$. And

$$I_L = I_C = \alpha I_E = \left(\frac{h_{FE}}{1 + h_{FE}}\right) I_E = \left(\frac{h_{FE}}{1 + h_{FE}}\right)\left(\frac{V_{cc} - v_1}{R_1}\right)$$

From the OAVR $v_1 = v_2 = v_{in}$. Thus

$$I_L = \left(\frac{h_{FE}}{1 + h_{FE}}\right)\left(\frac{V_{cc} - v_{in}}{R_1}\right) \tag{10.23}$$

The load current depends on the input voltage, V_{cc}, R_1, and h_{FE} of the transistor. We want I_L to be controlled by only v_{in}, so we want V_{cc}, R_1, and h_{FE} to be constant. It is easy to keep V_{cc} and R_1 constant, but h_{FE} will depend slightly on $I_C = I_L$. The best solution is to pick a transistor with a value of h_{FE} much greater than 1, so $h_{FE}/(1 + h_{FE}) \cong 1$. This means using a Darlington transistor for Q.

10.10 THE CURRENT-TO-CURRENT CONVERTER

An op amp can be used to multiply a current with the circuit of Fig. 10.11. The input voltage v_{in} is zero from the OAVR. Because the inverting input of the op amp draws negligible current (the OACR), the input current and the voltage v'_{out}, are simply related by Ohm's law:

$$i_{in} = \frac{-v'_{out}}{R_2}$$

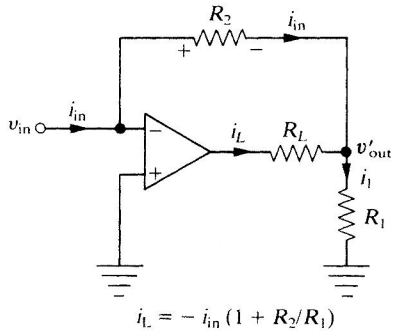


FIGURE 10.11 Current-to-current converter.

The KCL at the junction of R_L and R_1 implies

$$i_{in} + i_L = i_1 = \frac{v'_{out}}{R_1}$$

Using $v'_{out} = -i_{in}R_2$ yields

$$i_{in} + i_L = \frac{-i_{in}R_2}{R_1}$$

or

$$i_L = -i_{in}\left(1 + \frac{R_2}{R_1}\right) \tag{10.24}$$

Thus we see that the current through the load resistance is independent of R_L and depends only on the input current and the ratio R_2/R_1. Notice also that both ends of the load resistance must be floating above ground. A resistance can be placed in series with the noninverting input to minimize bias current effects on the output.

10.11 THE LOGARITHMIC AMPLIFIER

With the circuit of Fig. 10.12, we can use an op amp to produce an output voltage that is proportional to the logarithm of its input voltage. The qualitative explanation of the logarithmic amplifier is that as the input voltage goes more positive, the output of an op amp goes negative, which tends to turn on the npn transistor (the emitter going negative is equivalent to the base going positive). Thus, there is a smaller and smaller resistance (of the transistor) between the op amp output and the inverting input, which lowers the gain of the op amp. Thus, the larger the input signal voltage, the smaller the op amp gain, which effectively "compresses" the gain—a factor

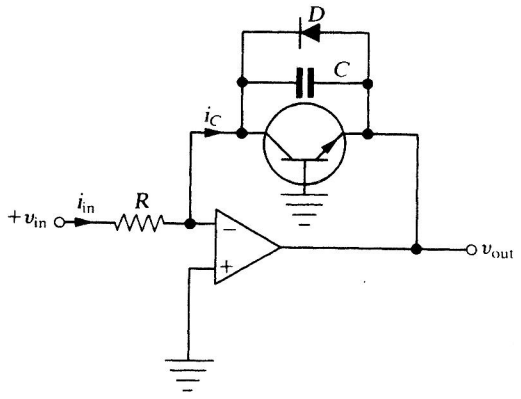


FIGURE 10.12 The logarithmic amplifier.

of 10 or 100 in the input will produce a much smaller factor in the output.

The KCL and the OACR applied to the junction at the inverting terminal imply $i_{in} = i_C$. The input current i_{in} can be expressed with Ohm's law, and the collector current of the transistor can be expressed in terms of its base emitter voltage.

$$i_C = \frac{v_{in} - 0}{R} = I_0 \, e^{eV_{BE}/kT}$$

But the base emitter voltage of the transistor is simply the negative of the output voltage: $V_{BE} = -v_{out}$. Thus,

$$\frac{v_{in}}{R} = I_0 e^{-ev_{out}/kT}$$

Solving for the output voltage, we obtain

$$v_{out} = -\frac{kT}{e} \ln\left(\frac{v_{in}}{I_0 R}\right) \qquad \textbf{(10.25)}$$

Using $v_{in} = +i_{in}R$, we can rewrite the output as

$$v_{out} = -\frac{kT}{e} \ln\left(\frac{i_{in}}{I_0}\right)$$

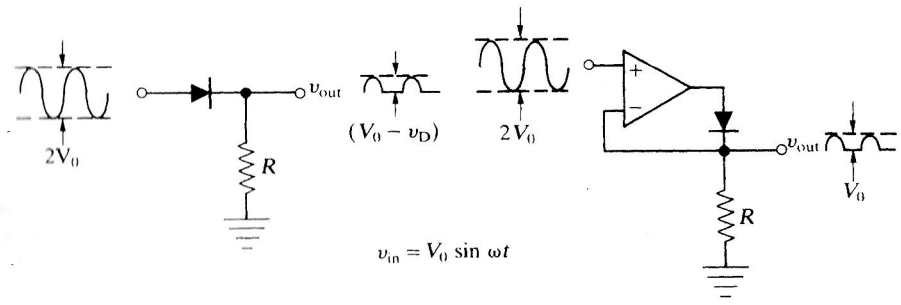
Notice:

1. The input voltage v_{in} must be positive (otherwise no current would flow through the transistor).

2. The output voltage range is limited to approximately −0.2 V to −0.7 V, because $v_{out} = V_{EB}$.
3. I_0 is usually about 100 pA or less because it is the reverse current for the transistor base-emitter junction and is temperature dependent.
4. The factor kT/e at room temperature is 0.026 V.
5. For small input currents i_{in} it is necessary to use an op amp with a bias current that is much smaller than the smallest i_{in}; this usually means an op amp with an FET input stage. For small input currents the input voltage v_{in} is also small, which means the output voltage due to input voltage offset may swamp the desired output; this means we must carefully null out the offset voltage with appropriate circuitry.
6. It is often necessary to add a small capacitance across the transistor to prevent oscillation as shown in Fig. 10.12.
7. When the op amp output goes positive (from a negative input), the npn transistor is turned off and the maximum collector emitter voltage may be exceeded. A diode is sometimes placed across the transistor to protect it as shown in Fig. 10.12.
8. If the input is a current source (with high impedance), the resistance R can be omitted—the high output resistance of the current source takes its place.

10.12 THE IDEAL DIODE

An ordinary silicon p-n junction diode does not pass an appreciable forward current until its forward voltage exceeds approximately $v_D = 0.5$ V, as shown in Fig. 10.13(a). However, if the diode is put in the feedback loop of an op amp, as shown in Fig. 10.13(b), the turn-on voltage of the diode is effectively reduced to $0.5 \text{ V}/A_o$, where A_o is the open-loop gain of the op amp. The qualitative explanation is that if the input voltage goes positive by only a slight amount (approximately v_D/A_o, where v_D is the diode turn-on voltage), the output of the op amp will go strongly positive and will turn on the diode. With the diode turned on the op amp circuit is essentially a voltage follower (see Section 10.3) with a gain of unity. Thus, the output

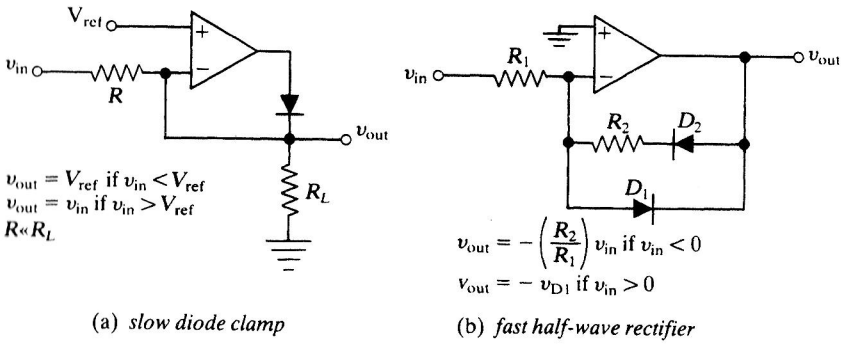


(a) *real diode half-wave rectifier* (b) *ideal diode half-wave rectifier*

FIGURE 10.13 The ideal diode.

equals the input, and the circuit acts like an ideal forward biased diode with almost zero turn-on voltage. But for a small negative input the op amp output will go strongly negative, thus turning the diode off. There is then no negative feedback, and the op amp output will saturate at close to the negative supply voltage $-V_{cc}$. The diode is then strongly reverse biased and the output of the circuit will be zero, because no current flows through R. Thus, the circuit acts like an ideal reverse biased diode.

An ideal diode clamp can be made with the circuit of Fig. 10.14(a). The



(a) *slow diode clamp* (b) *fast half-wave rectifier*

FIGURE 10.14 Diode clamp circuits.

noninverting input of the op amp is connected to a reference voltage. If the input voltage is less than the reference voltage, the op amp output goes positive, which turns on the diode. The output voltage is then equal to the reference voltage by the OAVR because the two inputs to the op amp must be the same. We say the output is *clamped* to the reference voltage, regardless of the input voltage, as long as the input is *less* than the reference voltage. But if the input voltage is greater than the reference voltage, then the op amp output goes strongly negative (approximately $-V_{cc}$), which turns off the diode. Thus, the output is proportional to the input because of the voltage divider action of R and R_L:

$$v_{out} = \frac{R_L v_{in}}{R + R_L} \cong v_{in}$$

If $R \ll R_L$, the output approximately equals the input. Notice also that as the input voltage goes below the reference voltage, the op amp output must go from $-V_{cc}$ to near V_{ref}, which can be 10 or 20 V, depending on V_{cc} and V_{ref}. Thus, the slew rate of the op amp may limit how fast the circuit can make this transition. For example, if the slew rate of the op amp is 2 V/μs, the op amp will take 9 μs for its output to swing from -13 V to $+5$ V. Thus to avoid distortion in the output, the input signal cannot change appreciably in 9 μs or a shorter time.

The circuit of Fig. 10.14(b) is a fast half-wave rectifier. If the input is negative, the op amp output is positive and D_2 is on and D_1 is off. Then we

have a standard inverting op amp, and $v_{out} = -(R_2/R_1)v_{in}$. If the input goes positive, the op amp output swings negative but only to -0.5 V (the drop across D_1); D_2 is off and D_1 is on. Then $v_{out} = -v_{D1}$ because the voltage at the inverting op amp input equals 0 by the OAVR. The circuit is thus a half-wave rectifier whose output is scaled by the factor $-R_2/R_1$. This circuit is faster because the output voltage swing is less.

An ideal full-wave rectifier can be made with the circuit of Fig. 10.15.

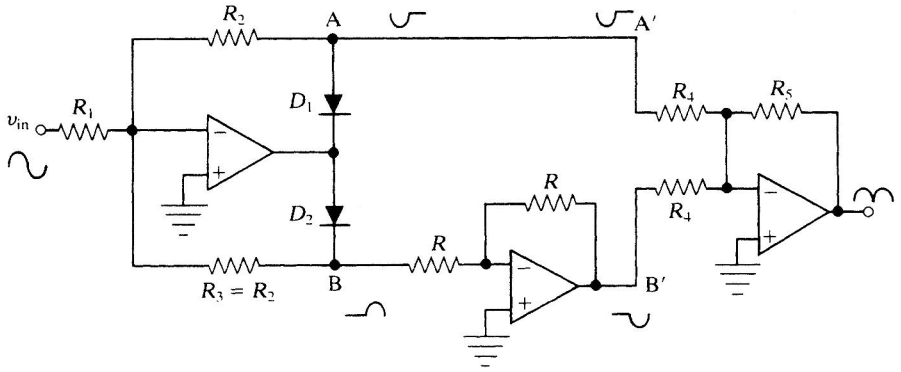


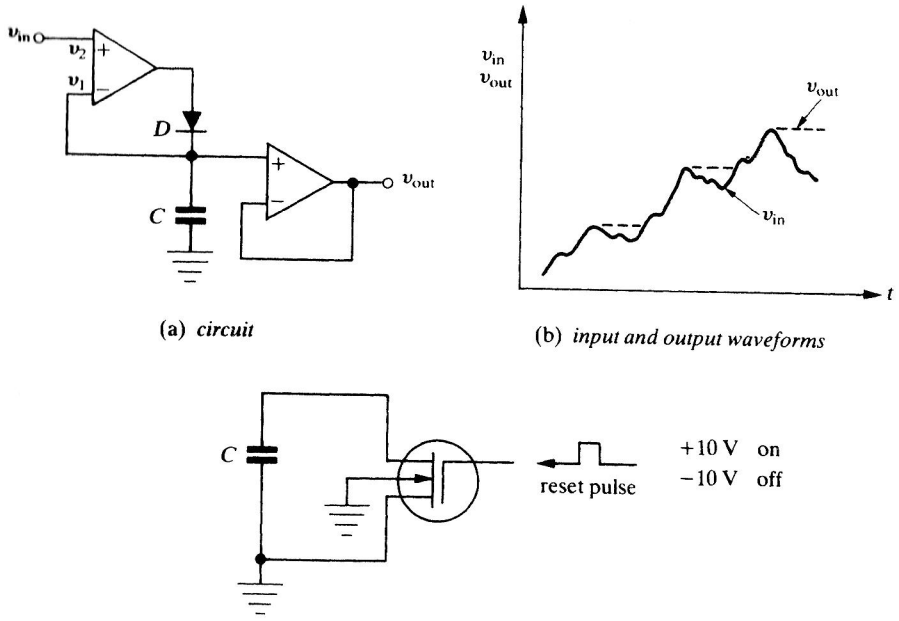
FIGURE 10.15 The ideal full-wave rectifier.

If the input is positive, the op amp output is negative; then D_1 is on and D_2 is off. Then we have a standard inverting op amp circuit, and the output is $v_A = -(R_2/R_1)v_{in}$. The output v_B is zero because there is no current through R_3. But if the input is negative, then the op amp output is positive and D_1 is off and D_2 is on. Again, we have a standard inverting op amp circuit, and the output is $v_B = -(R_3/R_1)v_{in}$, which is positive because v_{in} is negative. The output v_A is zero because there is no current through R_2. Thus, the positive part of the input appears as a negative voltage at output A, and the negative part of the input appears as a positive voltage at the output B.

An inverter amplifier with a gain of -1 in series with B will change the polarity of v_B. Then the two outputs at A′ and B′ are summed and inverted in sign by using a summing amplifier to produce the full-wave positive output. Then the output of the summer will be R_2R_5/R_1R_4 times the absolute value of the input; that is, the output will be that of a full-wave rectifier.

10.13 THE PEAK DETECTOR

If we add a high-quality capacitor to the output of the ideal half-wave rectifier of Fig. 10.13(b), let $R \to \infty$, and add a voltage follower, we have a peak detector as shown in Fig. 10.16(a). The output voltage will be stored



(a) *circuit*

(b) *input and output waveforms*

(c) *reset circuit*

FIGURE 10.16 Peak detector.

on the capacitor, and the voltage at the inverting input of the op amp will equal the output voltage $v_1 = v_{out}$. Thus if the input rises above v_{out}, the first op amp output will go more positive and turn on D, thus producing a voltage follower—the output voltage will follow the input voltage. The capacitance C will be charged through the diode by the op amp to the new more positive input voltage. But if the input voltage drops below v_{out}, the op amp output will fall and turn off D. Then the capacitance will be isolated and will hold its charge and voltage. The voltage on the capacitance is then fed into the input of a voltage follower. The discharge current from the capacitor will be the sum of the small reverse diode current and the bias current into the inverting input of the first op amp and the voltage follower.

If the input varies with time, then the output will rise to the most positive value of the input and hold there at the peak value until a more positive input comes along, as shown in Fig. 10.16(b). Notice:

1. The output voltage will droop (gradually decrease in time) as the capacitance discharges. To minimize this droop, use an op amp with a small input bias current (i.e., an FET op amp). The capacitance should also have a very high leakage resistance and low polarization, which usually means a polystyrene or silver mica capacitor must be used. The voltage follower op amp should also have a low input bias current, which means an FET op amp. The maximum droop rate is $dv_{out}/dt = I_B/C$, so a large capacitance is desirable.

2. The maximum rate of output change is limited by the slew rate of the op amp and by C.
3. The circuit can be reset by shorting out the capacitance. An FET switch can be used as shown in Fig. 10.16(c), but the switch must have an extremely high resistance when off. Thus, a MOSFET device would be appropriate. The positive reset pulse turns the MOSFET on and discharges the capacitor.
4. The output voltage change per unit time is limited by the current supplied by op amp 1.

$$\frac{dv_{out}}{dt} = \frac{d}{dt}\left(\frac{Q}{C}\right) = \left(\frac{1}{C}\right) I_{max}$$

where I_{max} is the maximum output current of the first op amp.

10.14 THE SAMPLE-AND-HOLD CIRCUIT

A circuit similar to the peak detector (Section 10.13) can be used to sample a waveform or pulse and store it for any desired length of time. This is particularly useful in analog-to-digital converters (covered in Chapter 15) where a voltage level at a certain time in an input analog waveform must be sampled and held for a period of time during which time the voltage level is converted into digital form. The circuit, shown in Fig. 10.17, uses a high-

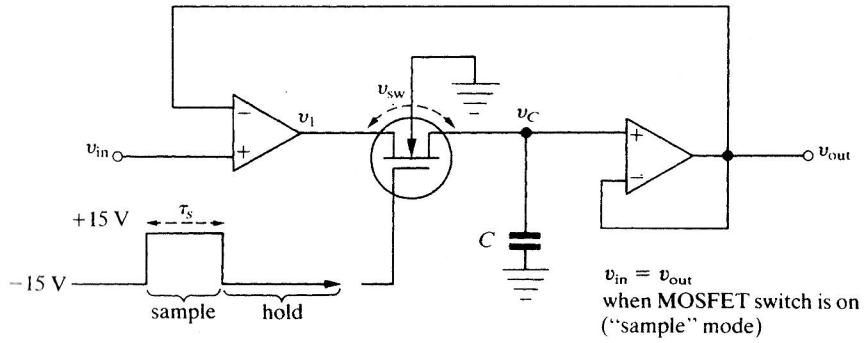


FIGURE 10.17 Sample-and-hold circuit.

input-impedance op amp at the input. When the MOSFET switch is "on" (from a positive voltage on its gate), the circuit is sampling the input, and $v_{out} = v_C \rightarrow v_{in}$ because the whole circuit acts like a voltage follower; that is, the capacitance is charged to the input voltage through the MOSFET. When the MOSFET is "off" the input voltage is "held" on the capacitor. The second voltage follower presents a high impedance across the capacitor, so the capacitor voltage does not decay appreciably before the next sample is taken. Notice:

1. The circuit samples the input for a time τ_s when the signal on the gate of the MOSFET is +15 V, thus turning the MOSFET on. The sampling time τ_s should be short enough so that the input signal does not change appreciably during τ_s. When the MOSFET gate voltage is at −15 V, the MOSFET is off and the circuit holds the input.
2. The bias current I_B of the second voltage follower must be small so that the capacitor does not discharge too quickly. The rate at which the capacitor voltage decreases or droops is

$$\frac{dV}{dt} = \left(\frac{1}{C}\right) I_B$$

so it is desirable to have I_B small and C large.
3. The capacitor charges through the series resistance of the "on" MOSFET, which is typically 50–100 Ω. Thus, the charging time constant is $RC \cong (100\ \Omega)(C)$, which should be smaller than the time during which the input signal changes appreciably. Thus, a small C is best. (The MOSFET resistance and C form a low-pass RC filter.)
4. The first voltage follower supplies the current to charge C. Because the current must be large enough to charge C quickly, the op amp output impedance should be small:

$$\frac{dV}{dt} = \frac{I_{out}}{C}$$

where I_{out} = the output current of the first op amp.
5. C should be high quality, and its leakage resistance should be large to avoid droop (polystyrene, teflon, or mica).

10.15 THE OP AMP DIFFERENTIATOR

An operational amplifier can be made to differentiate by using a capacitor and resistor feedback network, as shown in Fig. 10.18. Assume $C' = 0$ in the following explanation. Applying the KCL at the inverting input of the op amp yields

$$i_{in} = i_2 + i'$$

If we let Q be the charge on the capacitor C then $i_{in} = dQ/dt$. Neglecting i' as usual from the OACR and writing i_2 from Ohm's law yield

$$\frac{dQ}{dt} = \frac{v_1 - v_{out}}{R}$$

But $v_1 = v_2 = 0$ from the OAVR, which implies $Q = Cv_{in}$. Thus,

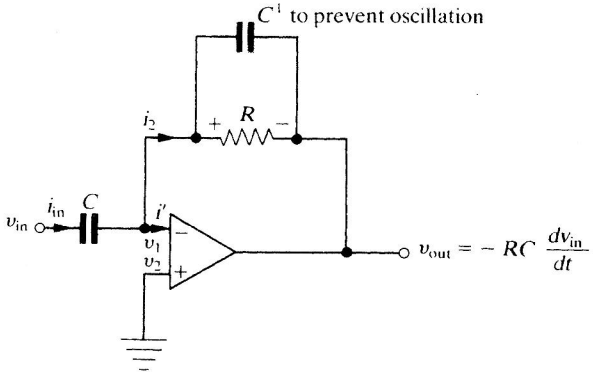


FIGURE 10.18 Op amp differentiator.

$$\frac{d(Cv_{in})}{dt} = -\frac{v_{out}}{R}$$

or

$$v_{out} = -RC\left(\frac{dv_{in}}{dt}\right) \qquad \textbf{(10.26)}$$

Notice that, unlike the passive RC differentiator of Chapter 3, we have made no assumptions about the input signal period compared to RC. In theory the op amp differentiator will work over a frequency range from dc to infinity, unlike the passive integrator of Chapter 3. In practice, of course, things are not so ideal. The differentiator tends to oscillate because its gain is so large at high frequencies. A practical cure for oscillation is a small capacitor C' connected across R to decrease the gain at high frequencies. The reactance of C' should be comparable to R at the frequency of oscillation. Sometimes a resistance in series with C is necessary.

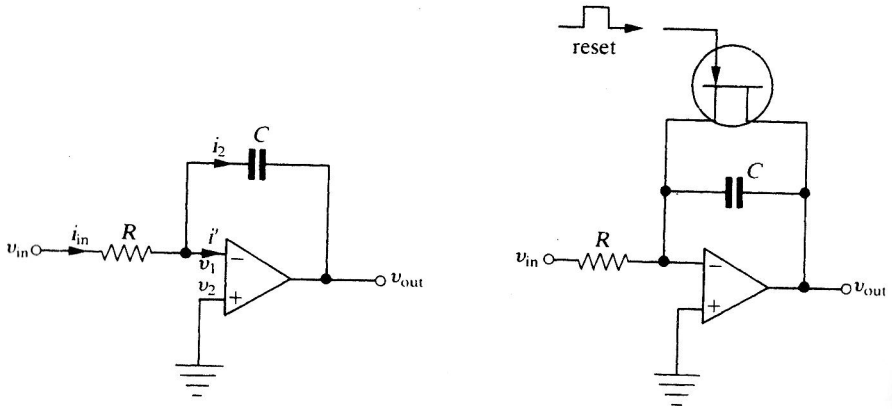
10.16 THE OP AMP INTEGRATOR

An op amp can be made to integrate by using the circuit of Fig. 10.19. Applying the KCL at the inverting terminal of the op amp yields

$$i_{in} = i_2 + i'$$

If Q is the charge on the capacitor, then $i_2 = dQ/dt$. By the OACR we can neglect i'. By Ohm's law $i_{in} = (v_{in} - v_1)/R$, and $v_1 = v_2$ from the OAVR, and $v_2 = 0$. Thus, we have

$$\frac{v_{in}}{R} = \frac{dQ}{dt}$$



(a) *basic circuit* (b) *with reset*

FIGURE 10.19 Op amp integrator.

But $Q = CV$, where V is the voltage across the capacitor, and $V = v_1 - v_{out} = -v_{out}$. Thus,

$$\frac{v_{in}}{R} = \frac{d(-Cv_{out})}{dt} = -C\left(\frac{dv_{out}}{dt}\right)$$

or

$$v_{out} = \frac{-1}{RC}\int v_{in}\, dt \qquad \textbf{(10.27)}$$

As in the case of the differentiator, notice that we made no assumptions about the input signal period compared with RC. Thus, in theory the op amp integrator will integrate over a frequency range from dc to infinity, unlike the passive RC integrator of Chapter 3. Notice:

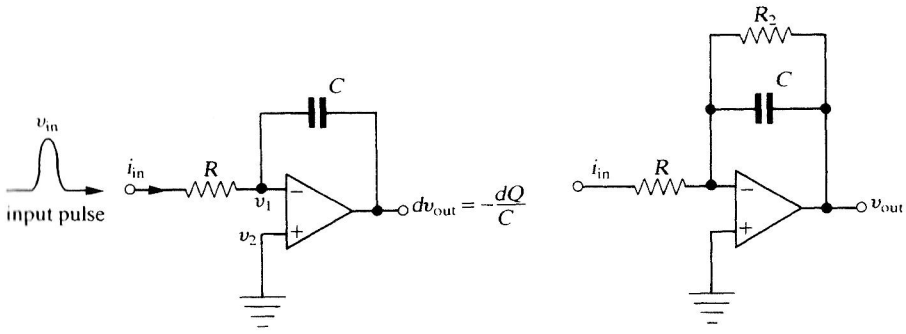
1. At the start of the integration we want the output to be zero, which requires that we start with no charge on the capacitor. Thus, there must be a shorting switch across C that should be opened when the integration is to start (i.e., when the input signal is applied). An FET switch can be used, as shown in Fig. 10.19(b). The signal to the gate that turns on the FET and shorts out C is called the *reset* signal. The time required to reset the integrator is about $R'C$, where R' is the "on" resistance of the FET channel, because C discharges through the FET.
2. If the input voltage is constant, $v_{in} = V_0$, then the output will be a negative-going linear ramp: $v_{out} = (-V_0/RC)t$.
3. $i_{in} = v_{in}/R$, so the output is proportional to the time integral of the input current: $v_{out} = -(1/C)\int i_{in}\, dt$.
4. There usually will be a long-term dc drift in the output of the integrator due to input offset effects, both voltage and current. For example, if V_{io} is the input offset voltage of the op amp, then V_{io} will be integrated by the integrator (if the capacitor is not shorted) and the output will be

$$v_{out} = \frac{-1}{RC}\int V_{io}\, dt$$

This drift also depends on the temperature because V_{io} depends on the temperature, typically 1–10 μV/°C. One cure is to use a large time constant RC, but this makes the output small for a real signal input. Another widely used cure is a resistance R_2 connected across C to bleed off the charge on C in a time of approximately R_2C. But this requires integrating the signal input in a time short compared to R_2C. Bias current effects can be reduced by using a low-bias-current FET op amp. Integrators, in general, are much better behaved than differentiators.

10.17 THE CHARGE-SENSITIVE AMPLIFIER

In some cases the signal source voltage remains essentially constant, and the source capacitance changes, such as in a capacitance microphone. Or the signal source emits a certain amount of charge dQ that must be detected, as in an X-ray proportional counter. What is required is a circuit to convert this charge dQ into an output voltage change; the amplifier to do this is called a *charge-sensitive amplifier*. The circuit of Fig. 10.20(a)



(a) *basic circuit* (b) *with R_2 to discharge C*

FIGURE 10.20 Charge-sensitive amplifier.

produces an output voltage change dv_{out} proportional to dQ. The circuit is basically an integrator. The op amp voltage rule implies $v_1 = v_2 = 0$. And the op amp current rule implies the input charge dQ all piles up on the capacitor plate. Thus

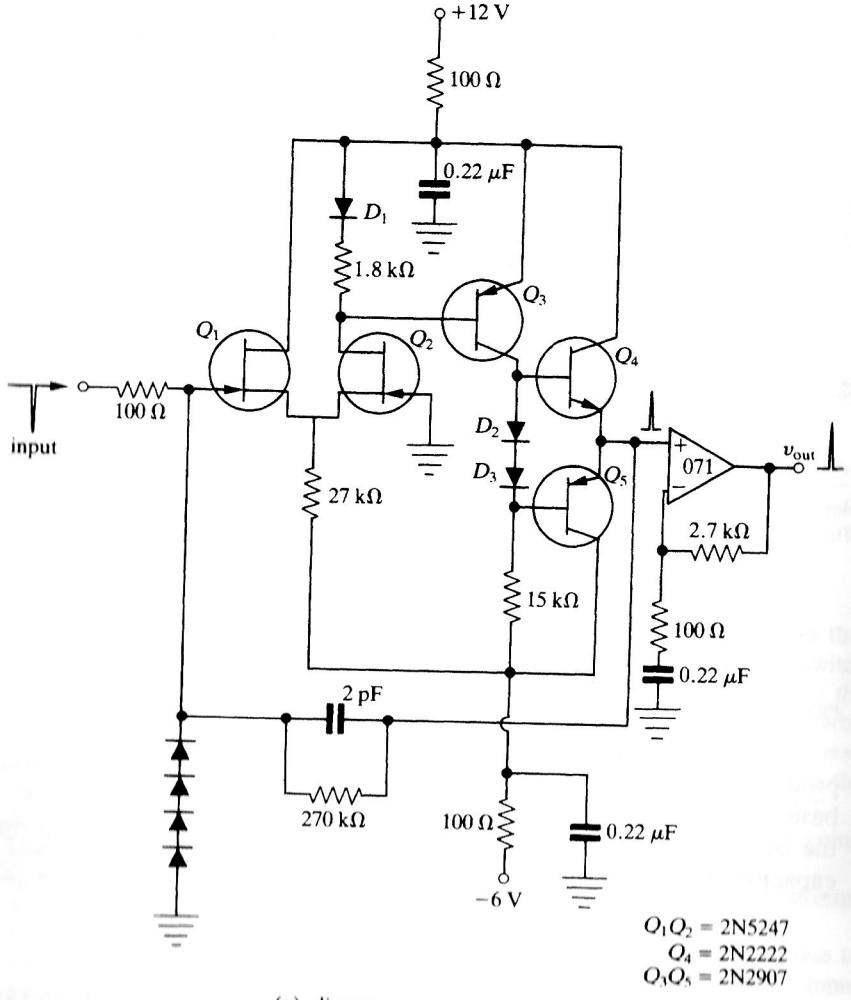
$$dQ = C(-\,dv_{out})$$

or

$$dv_{out} = -\frac{dQ}{C} \qquad \textbf{(10.28)}$$

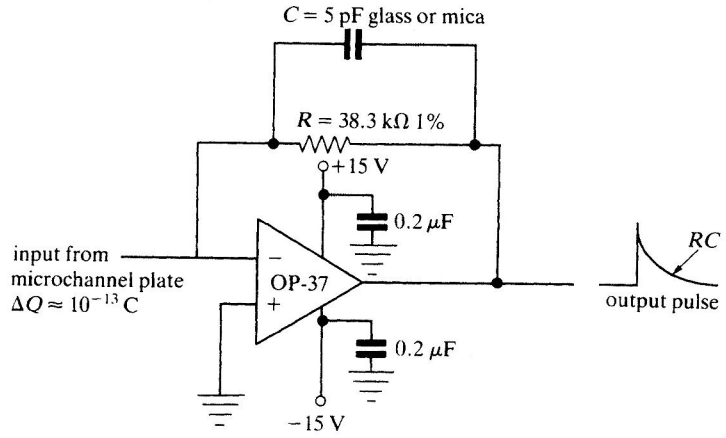
Thus the output voltage change is linearly proportional to the change in dQ. The smaller is C, the larger is the output voltage change for a given change in charge.

A little thought will show that as more and more input increments of charge come along, the output voltage steadily gets more and more negative until the op amp is saturated and its output voltage is near $-V_{cc}$. Thus, we must discharge the capacitor between the dQ inputs; to do so, we add a resistance R_2 in parallel with C, as shown in Fig. 10.20(b). R_2C limits the maximum counting rate, which must be less than $1/R_2C$. For example, if $R_2C = 1\ \mu$s ($C = 10$ pF, $R_2 = 100$ kΩ), the maximum rate of dQ events is approximately 1 MHz. For example, a plastic scintillator and photomultiplier tube will produce a 50-ns pulse input with $dQ = 24 \times 10^{-12}$ C = 24 pC. The output will then be a 4-V pulse with $C = 6$ pF. Commercial charge-sensitive amplifiers can detect charge increments $dQ = 0.16$ to 10 pC.

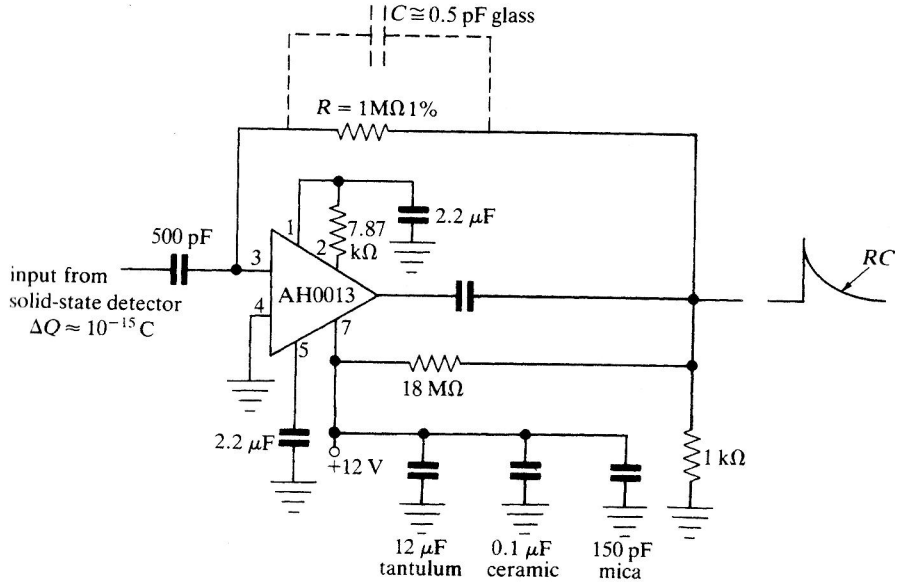


(a) *discrete component circuit*

FIGURE 10.21 Charge-sensitive amplifiers.



(b) *op amp circuit*



(c) *low-noise pre amp circuit*

FIGURE 10.21 Continued.

pulses from a photomultiplier (looking at a plastic scintillator) built from discrete components is shown in Fig. 10.21(a). The small, fast, negative input pulse is fed into the gate of one of the two FETs that are connected as a standard differential amplifier. The four diodes at the input provide protection against excessive input voltage. The diode D_1 in the drain of the other FET ensures that Q_3 is always biased "on." Q_3 is a common emitter amplifier and drives a push-pull output stage consisting of Q_4 and Q_5. Diodes D_2 and D_3 ensure that Q_4 and Q_5 are just barely conducting with no signal input. The output of the push-pull stage is amplified by a standard noninverting BIFET op amp. The integration of the input is due to the 2-pF capacitance from the emitters of Q_4 and Q_5 to the input and the 100-Ω resistance in series with the input. Two high-speed charge-sensitive amplifier circuits are shown in Figs. 10.21(b) and 10.21(c). The OP-37 op amp circuit is designed to amplify current pulses from a "microchannel plate." The AH0013 circuit is designed to amplify very small pulses from a solid-state electron detector. Notice the very careful bypassing of the +12-V supply; this is necessary for low noise operation.

The LeCroy TRA1000 charge-sensitive preamplifier comes as a 16-pin DIP (dual-in-line-package) and can also be used as a current-to-voltage converter. Its gain is 2.7 to 270 mV/μA or 100 to 500 mV/pC. Its noise can be as low as 0.1 fC (1 fC = 10^{15} C).

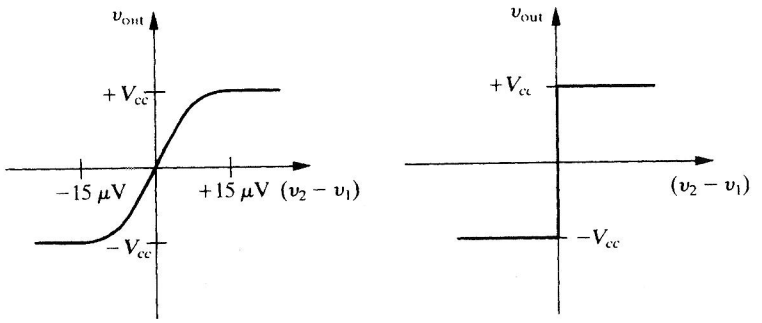
10.18 OP AMP COMPARATORS

The output of any op amp is always equal to the very large open-loop gain times the difference between the input voltage at the noninverting and inverting terminals of the op amp, provided the op amp is not saturated.

$$v_{out} = A_o(v_2 - v_1)$$

It is important to remember that v_2 and v_1 are the voltages at the op amp *terminals*, not the input voltages elsewhere in the circuit. The open-loop op amp gain is typically 10^5 to 10^6, and the maximum output voltage is the supply voltage V_{cc}, typically 15 V. Most bipolar op amp outputs can swing within 1–2 V of $\pm V_{cc}$; thus if $V_{cc} = 15$ V, the maximum output voltage might be 13 V. For discussion purposes we will assume the swing is to $\pm V_{cc}$. Thus, if the *differential* input is greater than 15 V/10^6 = 15 μV, the op amp output will be saturated at either +15 V or −15 V, depending on the polarity of the input. In other words, as the differential input slowly increases from a large negative value to a large positive value, the output suddenly changes from $-V_{cc}$ to $+V_{cc}$ as the input changes from −15 μV to +15 μV [see Fig. 10.22(a)]. An ideal comparator's response is shown in Fig. 10.22(b).

The time for the op amp to change from $-V_{cc}$ to $+V_{cc}$ is usually very short but is always limited by the slew rate of the op amp. Any op amp thus



(a) *actual comparator* $V_{cc} = 15$ V (b) *ideal comparator*

FIGURE 10.22 Comparator waveforms.

will essentially "compare" the two inputs at its two terminals and give either a large positive or a large negative output, provided its differential input exceeds approximately 15 μV. An op amp specially made to do this is called a *comparator*; it may switch its output from low to high in a very short time (as short as 50–100 ns) and may have a slew rate of up to 500 to 1000 V/μs. (An ordinary general-purpose op amp slew rate is approximately 1–5 V/μs.) This time to switch from $-V_{cc}$ to $+V_{cc}$ is called the *response time* of the comparator. One should bear in mind, however, that the faster the comparator, the more prone it is to unwanted oscillations, so unless a very short response time is essential to the circuit application, it may be better to use an ordinary op amp.

The comparator output can be restricted or clipped to values less than $\pm V_{cc}$ by connecting two zener diodes to the output as shown in Fig. 10.23(a). The maximum positive output voltage will be $V_D + V_{Z2}$, and the maximum negative voltage will be $-(V_D + V_{Z1})$, where V_D is the drop across the forward biased zener diode and V_Z is the zener voltage. One of the comparator inputs can be a fixed reference voltage, so the output will indicate when the input is greater than or less than the reference voltage, as shown in Fig. 10.23(b).

Some comparators have *open collector* outputs, which means one must wire an external resistor from the output to a positive supply voltage, as shown in Fig. 10.23(c). Then the output is either $+V_{cc}$ when Q is off or approximately 0.2 V when Q is strongly on (saturated). This circuit is useful in digital applications where the two logic levels are 3.5 V and 0.2 V.

If the input changes slowly, the comparator output should flip suddenly when the differential input voltage goes through zero. But if the input is noisy, the differential input may change sign several times in a short time interval as the overall dc input level changes sign; in other words, the comparator output will flip back and forth several times from $+V_{cc}$ to $-V_{cc}$ instead of making just one flip. The output will then contain a brief burst of

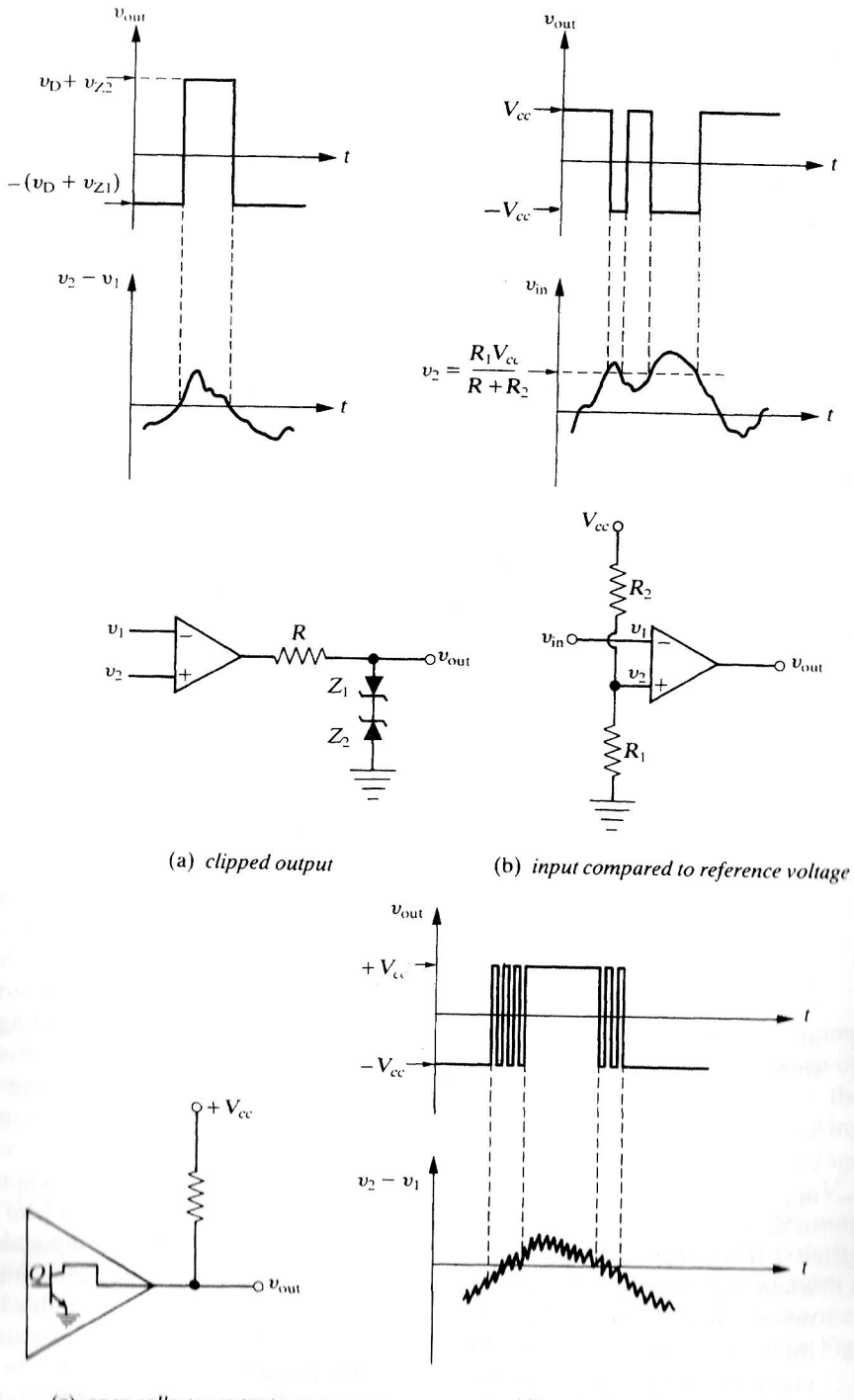


FIGURE 10.23 Comparators.

large "noise" pulses, as shown in Fig. 10.23(d), that may wreak havoc with the rest of the circuit. To avoid this, we need less noise on the input signal, a slower comparator, or a circuit that flips its output up when the differential input goes 15 μV positive but flips back when the differential input goes several tenths (or more) of a volt negative—a circuit that has a different input voltage threshold for a positive output flip compared to a negative output flip. This behavior is called *hysteresis*, and the Schmitt trigger circuit of Section 10.19 solves the problem.

A simple comparator application is shown in Fig. 10.24; when the

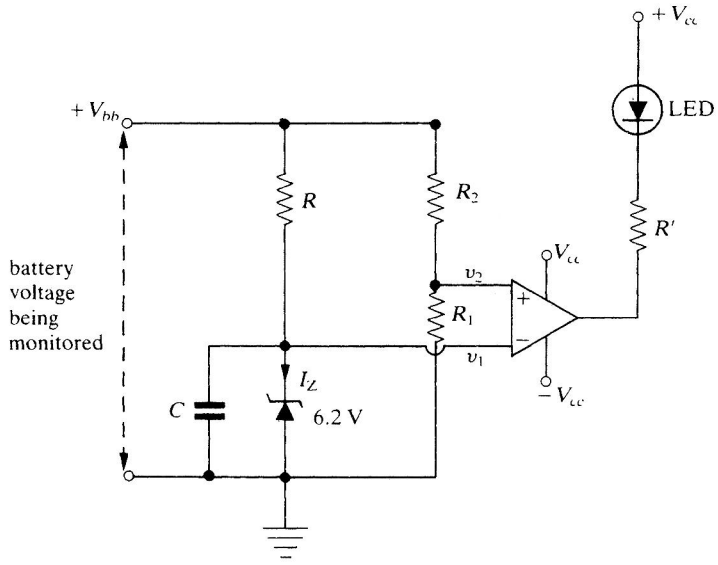


FIGURE 10.24 Low-battery indicator.

battery voltage drops below a certain value determined by R_1 and R_2, the op amp comparator output goes low and turns on the LED. The comparator inputs are

$$v_2 = \frac{R_1}{R_1 + R_2} V_{bb} \quad \text{and} \quad v_1 = 6.2 \text{ V (the zener voltage)}$$

Under normal operation with a good battery $v_2 > v_1$, the op amp output is high (V_{cc}), and the LED is out. When V_{bb} decreases to the value where $v_2 < v_1$, then the op amp output goes low ($-V_{cc}$), which turns on the LED. For example, if the battery voltage is $V_{bb} = 13.2$ V when fully charged (a "12"-V auto battery) and if we desire the LED to go on when V_{bb} falls to 12 V, then we choose R_1 and R_2 so that $v_2 = 6.2$ V when $V_{bb} = 12$ V. Thus

$$\frac{v_2}{V_{bb}} = \frac{6.2\text{ V}}{12\text{ V}} = \frac{R_1}{R_1 + R_2} = 0.517$$

Hence,
$$1 + \frac{R_2}{R_1} = \frac{1}{0.517} = 1.934 \quad \text{or} \quad \frac{R_2}{R_1} = 0.934$$

R is chosen so that the zener diode conducts approximately $I_Z = 1$–2 mA. Thus

$$I_Z R \cong V_{bb} - V_Z$$

or
$$R \cong \frac{V_{bb} - V_Z}{I_Z} = \frac{13.2\text{ V} - 6.2\text{ V}}{2\text{ mA}} \cong 3.5\text{ k}\Omega$$

R' is chosen so that the LED is brightly on when the op amp comparator output is low ($-V_{cc}$), which occurs for a current of 10 mA for most LEDs. The voltage drop across a lighted LED is approximately 1.5 V, so

$$1.5\text{ V} + I_{\text{LED}}R' = V_{cc} - (-V_{cc})$$

$$R' = \frac{2V_{cc} - 1.5\text{ V}}{I_{\text{LED}}}$$

$$R' = \frac{28.5\text{ V}}{I_{\text{LED}}} = \frac{28.5\text{ V}}{10\text{ mA}} \cong 2.8\text{ k}\Omega$$

A capacitance C across the zener diode might be necessary to prevent noise from flipping the comparator. Finally, we note that a slow comparator (i.e., an ordinary op amp) would work fine in this application.

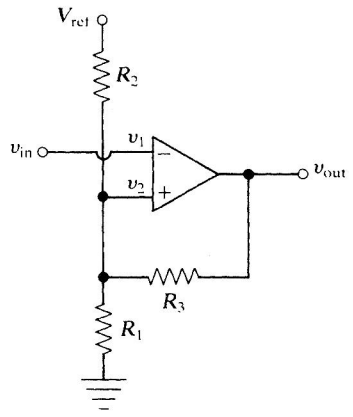
10.19 THE SCHMITT TRIGGER

If we tie the output of the comparator to the noninverting input, as shown in Fig. 10.25(a), then the voltage at this input v_2 will depend on the output. If the output is high, v_2 will be higher than it will be when the output is low; this produces hysteresis. The voltage at which the comparator flips depends on the "history" of the circuit—whether the circuit output was previously high or low.

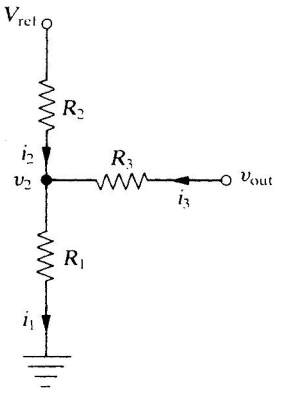
A quick numerical calculation should make the point clear. From Fig. 10.25(b), the KCL implies

$$i_2 + i_3 = i_1$$

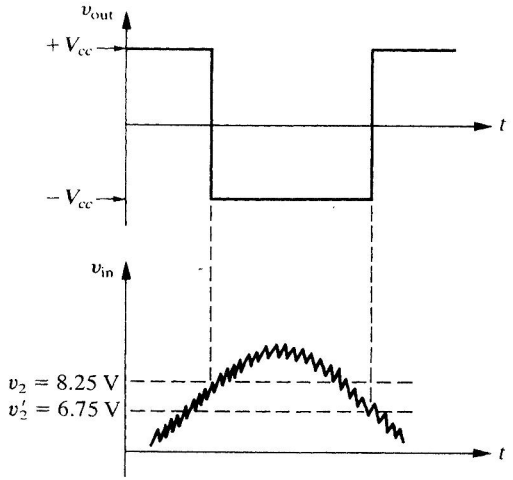
$$\frac{V_{\text{ref}} - v_2}{R_2} + \frac{v_{\text{out}} - v_2}{R_3} = \frac{v_2}{R_1}$$



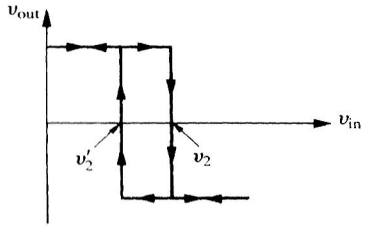
(a) *basic circuit*



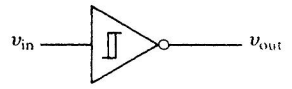
(b) *voltage divider circuit*



(c) *waveforms for* $R_1 = R = 1\text{ k}\Omega$, $R_3 = 10\text{ k}\Omega$, $V_{cc} = 15$ V



(d) *input-output hysteresis curve*



(e) *simple Schmitt trigger circuit symbol*

FIGURE 10.25 The Schmitt trigger.

or $$\frac{V_{ref}}{R_2} + \frac{v_{out}}{R_3} = v_2\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) = \frac{v_2}{R_{123}}$$

where $$R_{123} = \frac{R_1R_2R_3}{R_1R_2 + R_1R_3 + R_2R_3}$$

is the parallel combination of R_1, R_2, and R_3. Thus,

$$v_2 = \frac{R_{123}}{R_2} V_{ref} + \frac{R_{123}}{R_3} v_{out} \tag{1}$$

Remember, v_2 is the threshold voltage; if $v_{in} = v_1$ is greater than v_2, the comparator flips low; if v_{in} is less than v_2, the comparator flips high. We immediately see from (1) that the threshold voltage depends on v_{out}. If the output is high, $v_{out} = V_{cc}$, and

$$v_2 = \frac{R_{123}}{R_2} V_{ref} + \frac{R_{123}}{R_3} V_{cc} \tag{2}$$

If the output is low, $v_{out} = -V_{cc}$ and

$$v_2' = \frac{R_{123}}{R_2} V_{ref} - \frac{R_{123}}{R_3} V_{cc} \tag{3}$$

The difference in the threshold voltages is

$$v_2 - v_2' = \frac{2R_{123}}{R_3} V_{cc} \tag{4}$$

If $R_1 = R_2 = R$, then

$$v_2 = \frac{R_3}{R + 2R_3} V_{ref} + \frac{R}{R + 2R_3} V_{cc} \cong \frac{V_{ref}}{2} + \frac{R}{2R_3} V_{cc}$$

and $$v_2' = \frac{R_3}{R + 2R_3} V_{ref} - \frac{R}{R + 2R_3} V_{cc} \cong \frac{V_{ref}}{2} - \frac{R}{2R_3} V_{cc}$$

where we have assumed $R \ll R_3$. The difference in the threshold voltage is then

$$v_2 - v_2' \cong \frac{R}{R_3} V_{cc} \tag{10.29}$$

If $V_{ref} = V_{cc} = 15$ V, $R_1 = R_2 = R = 1$ kΩ, and $R_3 = 10$ kΩ, then

$v_2 = 8.25$ V $\quad v_2' = 6.75$ V $\quad v_2 - v_2' = 1.5$ V

Thus, if the output is already high, $v_2 = 8.25$ V, and the input voltage is low and increasing, it must exceed 8.25 V to flip the comparator output to low. If the output is already low, $v_2' = 6.75$ V, and the input voltage is high and decreasing, it must fall below 6.75 V to flip the comparator output to high. If the input goes up to 8.3 V (the output will flip low) and then a noise pulse decreases the input below 8.25 V, the comparator will *not* flip back high. The net effect is to make the comparator insensitive to small amplitude noise in the input, provided the peak-to-peak noise amplitude is less than the difference in the triggering levels. Thus the noise pulses in the output are eliminated as the input passes through the threshold voltage. The waveforms are shown in Fig. 10.25(c) for a comparator with hysteresis. Without hysteresis the waveform is that of Fig. 10.23(d). The input-output voltage graph is shown in Fig. 10.25(d), and a simple Schmitt trigger circuit symbol is shown in Fig. 10.25(e). The open circle at the output means the output is inverted compared to the input. The use of a Schmitt trigger is extremely common in "cleaning up" noisy signals.

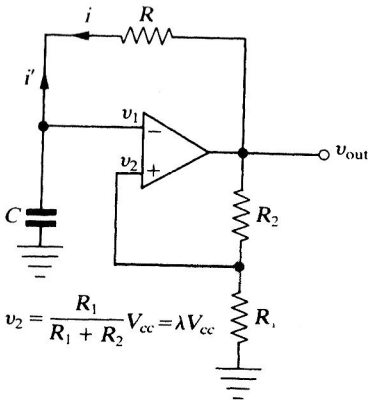
10.20 THE SQUARE-WAVE GENERATOR OR ASTABLE MULTIVIBRATOR

If the output of a comparator is fed back to its two inputs, we can make a square-wave oscillator or *astable* multivibrator, as shown in Fig. 10.26(a). Because of the feedback from the output to the noninverting input through R_1 and R_2, the voltage at the noninverting input of the op amp is always equal to

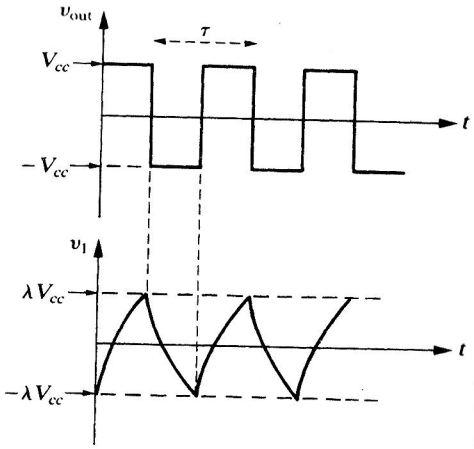
$$v_2 = \frac{R_1}{R_1 + R_2} v_{out} \equiv \lambda v_{out}$$

Thus, the circuit is like the Schmitt trigger circuit in that the "reference" voltage v_2 at the noninverting input depends on the output. Thus, as the capacitor C charges and discharges, the comparator action of the op amp will flip the output at a voltage depending on the output voltage. Let us assume that C is uncharged ($v_1 = 0$) and $v_{out} = +V_{cc}$. C will then charge up from i flowing through R ("toward" V_{cc}) with a time constant RC. The output will flip from $+V_{cc}$ to $-V_{cc}$ when C charges to $v_1 = v_2 = \lambda V_{cc}$. When the output flips to $-V_{cc}$, v_2 will immediately change to $-\lambda V_{cc}$ and C will start discharging from i' flowing through R ("toward" $-V_{cc}$) with a time constant RC. When v_1 reaches $v_2 = -\lambda V_{cc}$, the output will flip from $-V_{cc}$ to $+V_{cc}$. The waveforms for v_1 (on C) and v_{out} are shown in Fig. 10.26(b). The output is a square wave.

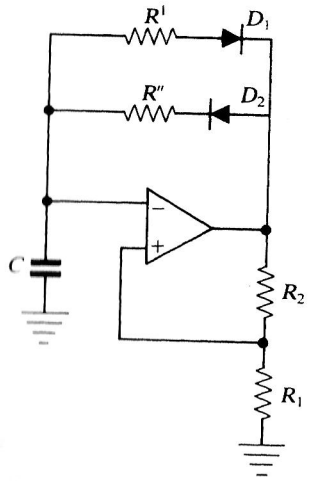
An analysis of the charging and discharging waveforms shows that the period is given by



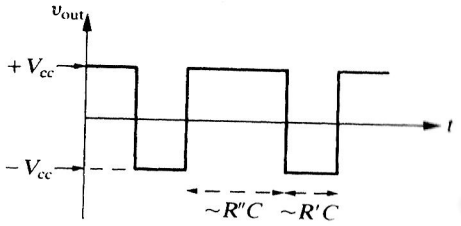
(a) *circuit for symmetric output*



(b) *waveforms*



(c) *circuit for asymmetric output*



(d) *output waveform for $R'' > R'$*

FIGURE 10.26 Square-wave generator.

$$T = 2RC \ln\left[\frac{1+\lambda}{1-\lambda}\right] \quad \text{where } \lambda = \frac{R_1}{R_1 + R_2} \tag{10.30}$$

Notice:

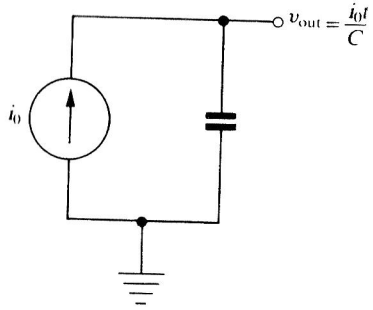
1. The period is independent of the output amplitude; the period depends only on R, C, R_1, and R_2.
2. The bias current of the op amp should be less than the charging and discharging current of C.

The output square wave can be made asymmetrical by having the capacitor C charge and discharge with different time constants. The circuit of Fig. 10.26(c) accomplishes this with the two diodes. When the output is high, diode D_2 will be on and diode D_1 will be off. Thus, C will charge through R'' with a time constant $R''C$, and the output will be high for approximately $R''C$ seconds. When the output is low, diode D_1 will be on and diode D_2 will be off. Then C will discharge through R' with a time constant $R'C$, and the output will be low for approximately $R'C$ seconds. The waveform output for $R'' > R'$ is shown in Fig. 10.26(d).

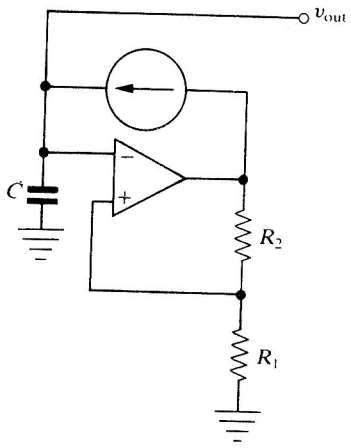
For both the symmetrical and the asymmetrical circuits the output has to change from a large positive voltage (V_{cc} or near V_{cc}) to a large negative voltage ($-V_{cc}$ or near $-V_{cc}$) in a time short compared to the period of the square wave. Thus, the slew rate of the op amp must be large enough to accomplish this. If the slew rate is not large enough, the output will not be square—there will be appreciable rise and fall time, and at higher frequencies the output will be rounded off into an approximately triangular shape. For an inexpensive op amp with a slew rate of $1.0\ \text{V}/\mu\text{s}$, the maximum square-wave output frequency is approximately 10 kHz.

10.21 THE TRIANGLE-WAVE GENERATOR OR RAMP GENERATOR

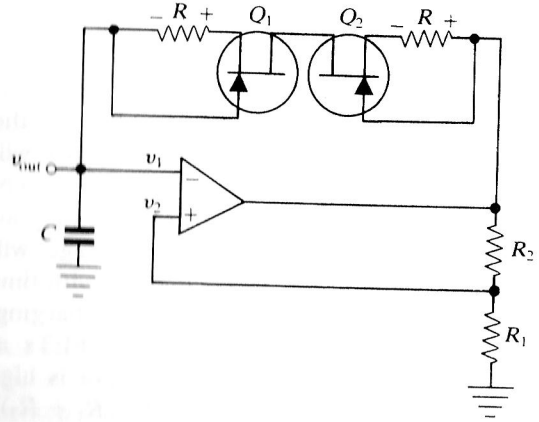
A linearly increasing voltage or *ramp* can be produced if a capacitance C is charged with a constant current, as shown in Fig. 10.27(a). If i_0 is the constant charging current, then the (output) voltage on the capacitance will be $V_C = Q/C = i_0 t/C$, where t is the time. If we add a constant current source to the square-wave generator circuit of Fig. 10.26 so that it supplies the charging current to the capacitor, then the capacitor voltage will increase linearly with time as it charges and will decrease linearly with time as it discharges. The basic circuit is shown in Fig. 10.27(b) for C charging, and the constant current sources are realized with n-channel JFETs as shown in Fig. 10.27(c). Assume the op amp (comparator) output is high (V_{cc}) and there is zero charge on C. Then $v_2 = \lambda V_{cc}$ [$\lambda = R_1/(R_1 + R_2)$], and $v_1 = v_C$ increases as C charges through the two FETs. With a high op amp output, Q_2 conducts strongly because its gate is positive with respect to its source; that is, Q_2 acts like a low resistance of several hundred ohms. But Q_1 acts like a constant current source because its gate is negative with respect to its source (see Fig. 6.4 for typical FET curves). C continues to charge linearly until $v_C = v_2 = \lambda V_{cc}$, at which point the output flips to $-V_{cc}$. Then C will discharge linearly through the two FETs with a constant discharge current. As C discharges, Q_1 is strongly on and Q_2 acts like a constant current source. When v_C decreases to $-\lambda V_{cc}$, the output flips high and C starts to charge linearly. Thus, the output on the capacitor will be a ramp or a sawtooth waveform as shown in Fig. 10.27(d).



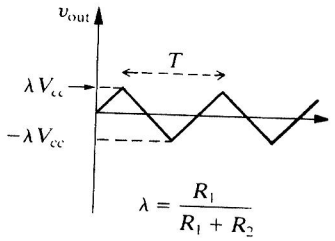
(a) *basic circuit*



(b) *C charging*



(c) *complete circuit*



(d) *output waveform*

FIGURE 10.27 Ramp generator.

One-half the period of the sawtooth will be the time it takes C to charge from $-\lambda V_{cc}$ to $+\lambda V_{cc}$. If we let i_0 be the charging current, then

$$i_0 = \frac{dQ}{dt} = \frac{d}{dt}(CV_C) = C\frac{dV_C}{dt} = C\left(\frac{2\lambda V_{cc}}{\frac{T}{2}}\right)$$

Solving for T gives

$$T = \frac{4\lambda C V_{cc}}{i_0} \quad \text{and} \quad f = \frac{1}{T} = \frac{i_0}{4\lambda C V_{cc}} \tag{10.31}$$

Notice:

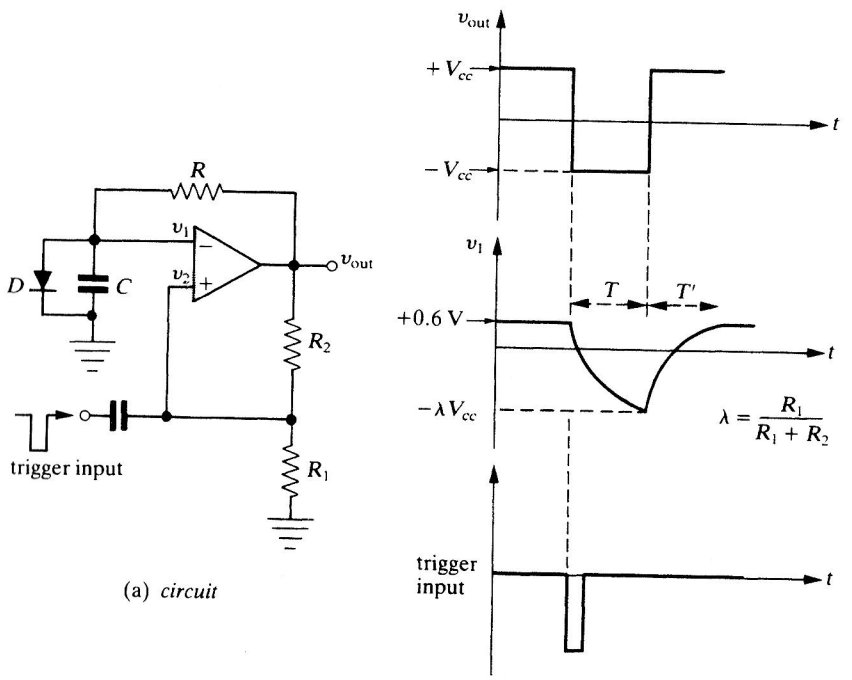
1. The period depends not only on the capacitance C, the resistances R_1 and R_2, and the charging current (determined by the FETs), but also on the magnitude of the supply voltage V_{cc}.
2. For equal positive and negative slopes on the sawtooth output waveform, the two FETs should be matched.
3. The $i_0 R$ drop must be large enough to pinch off the FET—that is, large enough to ensure that the FET is operating on the constant current portion of its I_D-versus-V_{DS} curve.
4. The bias current of the op amp should be less than i_0.

10.22 THE MONOSTABLE MULTIVIBRATOR OR ONE SHOT

A monostable multivibrator has only one stable state and one unstable or transient state. The circuit normally sits in the stable state until a trigger pulse comes along and flips it into its unstable state. It remains in the unstable state for a fixed time, depending on the circuit time constant, and then it automatically flips back into its stable state. The output voltages for the stable and unstable states are different, so the output voltage changes for a time interval depending on the circuit time constant. Thus, in a monostable multivibrator one input trigger pulse (usually short) produces one output pulse whose width depends on the circuit time constant RC.

If we add a diode in parallel with the capacitance of the square-wave generator of Fig. 10.26, we have the monostable multivibrator circuit in Fig. 10.28. The voltage v_1 at the inverting input of the op amp can never be more positive than the diode turn-on voltage, about 0.6 V. If we choose R_1 and R_2 so that $v_2 = \lambda V_{cc} = (R_1/(R_1 + R_2))\, V_{cc} > 0.6$ V, then the noninverting input will be more positive than the inverting input and the op amp output will be $+V_{cc}$. This is the stable state: $v_1 = v_C = 0.6$ V, and $v_{out} = +V_{cc}$.

If we feed in a negative trigger pulse through a capacitor to the noninverting input, then, if v_2 is driven below v_1, the op amp will flip the output to the low state: $v_{out} = -V_{cc}$. For the op amp to do this, the trigger pulse must be larger in amplitude than $\lambda V_{cc} - 0.6$ V. When the op amp flips its output low, v_2 is changed from $+\lambda V_{cc}$ to $-\lambda V_{cc}$. The capacitor, which was initially at 0.6 V, will now discharge through R towards the $-V_{cc}$ voltage at the output, and v_1 will become more negative, thus reverse biasing the diode. C will discharge until v_1 reaches $v_2 = -\lambda V_{cc}$, at which point the output will



(a) *circuit*

(b) *waveforms; T' = dead time*

FIGURE 10.28 Negative output monostable multivibrator.

flip back to the stable state of $v_{out} = +V_{cc}$. The time it takes C to discharge depends on the time constant RC. As soon as the output flips up to $+V_{cc}$, the capacitor starts charging until $v_1 = 0.6$ V. During this charging time T' (or recovery time or *dead time*), the circuit is generally unable to respond to a trigger pulse unless the trigger pulse is much larger than $\lambda V_{cc} - 0.6$ V.

It can be shown that the time the output remains low is given by

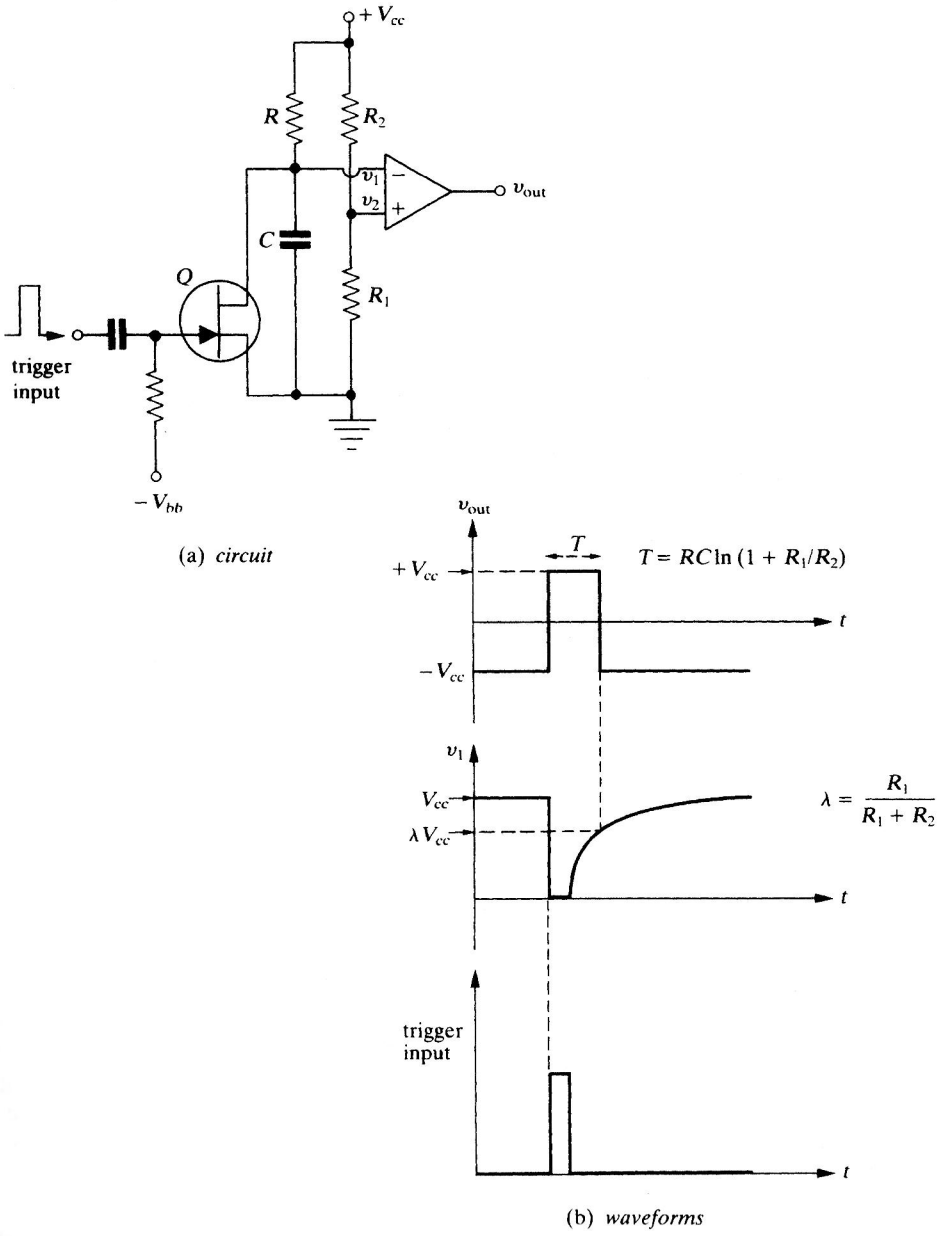
$$T = RC \ln \frac{1 + \dfrac{V_D}{V_{cc}}}{1 - \lambda} = RC \ln \left[\frac{V_{cc} + V_D}{V_{cc}(1 - \lambda)} \right] \qquad \textbf{(10.32)}$$

and the recovery time is

$$T' = RC \ln \frac{V_{cc}(1 + \lambda)}{V_{cc} - V_D}$$

where V_D is the diode forward voltage. If we make $\lambda \ll 1$ ($R_1 \ll R_2$), then $T' \ll T$, and the recovery time is short compared to the length of the output pulse.

A monostable multivibrator with a positive output pulse and no dead time is shown in Fig. 10.29(a). In the stable state the FET is normally biased off by $-V_{bb}$, and the voltage at the noninverting input is $v_2 = (R_1/(R_1 + R_2))V_{cc} = \lambda V_{cc}$. The output is normally low because the invert-



(a) *circuit*

(b) *waveforms*

FIGURE 10.29 Positive output monostable multivibrator.

ing input voltage v_1 equals V_{cc} because C has charged up to V_{cc} through R. When a positive trigger pulse comes in, the FET is turned on briefly, which quickly discharges C through the FET to ground, thus lowering the voltage v_1 at the inverting input from V_{cc} to near ground. Thus, the trigger pulse makes v_1 less than v_2, which causes the comparator to flip the output to high ($+V_{cc}$). At the end of the trigger pulse, the FET is turned off again, which allows C to charge again through R with a time constant RC. When C charges to λV_{cc}, the comparator flips the output back to its normal low state. The waveforms are shown in Fig. 10.29(b). It can be shown that the width of the output pulse is

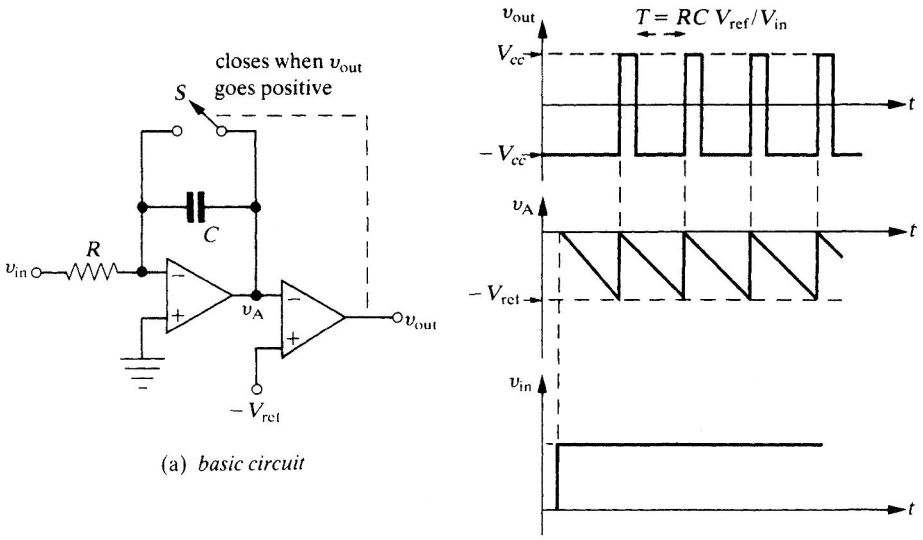
$$T = RC \ln\left(1 + \frac{R_1}{R_2}\right) \qquad \textbf{(10.33)}$$

The FET must be turned on strongly enough so that rC is less than the width of the trigger pulse, where r is the "on" resistance of the FET. This is to ensure that C discharges to below λV_{cc} while the trigger pulse is on. There is no dead time in this circuit; a new trigger pulse will cause a new output pulse at any time after the fall of the first output pulse.

10.23 THE VOLTAGE-CONTROLLED OSCILLATOR

A *voltage-controlled oscillator* (VCO) is a device that converts an input analog voltage into a series of pulses or waveforms whose frequency is linearly proportional to the magnitude of the input voltage. Another name is a *voltage-to-frequency converter* (V/F). The output waveform is typically a series of narrow pulses; the pulse repetition rate or pulse frequency is linearly proportional to the input voltage. VCOs are presently available on a chip for several dollars. The basic circuit, shown in Fig. 10.30(a), consists of an integrator followed by a comparator.

The circuit operation is as follows: Assume that the capacitor is uncharged and that a positive input voltage is applied. The input is integrated, and the output v_A of the integrator goes negative according to $v_A = -(1/RC) \int v_{in}\, dt$, as shown in Fig. 10.30(b). The noninverting input of the comparator is held constant at a negative reference voltage, so the comparator output is initially low. When the integrator output v_A drops below this negative reference voltage, the comparator output will flip high. But this high comparator output lasts only a very short time, because it closes the switch (a transistor) across C, which immediately discharges C and causes v_A to drop to zero, thus flipping the comparator output back to its initial low state. The resulting comparator output is a narrow positive pulse. The switch opens as soon as the comparator output goes low, the integrator starts integrating the input once more, and the process repeats itself. The larger the input voltage, the less time is taken for the integrator



(a) *basic circuit*

(b) *waveforms*

FIGURE 10.30 Voltage-controlled oscillator.

output to fall from zero to the negative reference voltage, and the shorter the time between the output pulses—in other words, the output pulse frequency is higher.

If we let T be the time for the integrator output to go from 0 to $-V_{ref}$, then, since the integrator output is the voltage on C, we have

$$-V_{ref} = \frac{-1}{RC} \int_0^T v_{in}\, dt = \left(\frac{-1}{RC}\right) v_{in} T$$

and

$$T = \frac{RCV_{ref}}{v_{in}}$$

Thus the output frequency is

$$f = \frac{1}{T} = \frac{v_{in}}{RCV_{ref}} \qquad \textbf{(10.34)}$$

which is linearly proportional to the input voltage. This assumes that the integrator is a true integrator. Notice:

1. The integrator output must go below the negative reference voltage to flip the comparator.
2. The time to discharge the capacitor through the transistor switch should be negligible compared to the pulse period T.

3. The narrow output pulses can be shaped by a monostable multivibrator as described in Section 10.22.
4. If the input voltage changes during the time T, the output frequency will be proportional to the average input voltage during the time T.
5. If the dc input voltage is derived from the same reference voltage, then the ratio v_{in}/V_{ref} will be independent of drifts in the reference voltage.

This circuit is useful for converting an analog signal into digital form, as we will see in Chapter 15.

10.24 SINE-WAVE OSCILLATORS

A number of different sine-wave oscillators can be made with op amps. The basic idea behind any oscillator is to provide positive feedback and to have the open-loop gain times the feedback fraction greater than or equal to unity: $A_oB \geqq 1$. If the feedback is positive for many frequencies, a non-sinusoidal output will be produced, such as in a square-wave oscillator (astable multivibrator). But if positive feedback occurs only at one frequency (or over a narrow band of frequencies), then a sinusoidal output will result at that one frequency if $A_oB \geqq 1$.

10.24.1 Phase-Shift Oscillator

To produce positive feedback, we must make the phase of the feedback signal equal to the phase of the input signal. If the input signal is at the inverting input of an op amp, the output will be 180° out of phase with respect to the input. Thus, for positive feedback we must produce another 180° of phase shift of the op amp output before feeding it back to the inverting input. One way to do this is to feed the op amp output into three simple RC filters, each of which produces an average phase shift of 60°; this produces a total 180° phase shift in the RC network and a total phase shift of 360°, which means positive feedback. The circuit is shown in Fig. 10.31.

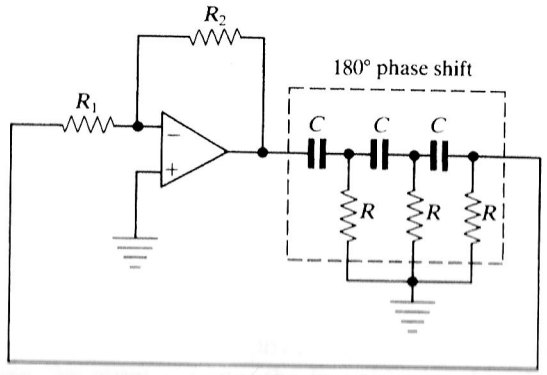


FIGURE 10.31 Phase-shift oscillator.

It can be shown that the RC network produces a total 180° phase shift at only one frequency: $f = 1/2\pi\sqrt{6}\ RC$. At this frequency the feedback fraction $B = 1/29$. Thus, the gain of the circuit must be at least 29 for oscillation. The gain is determined by R_2 and R_1, so these resistances usually are chosen to produce oscillation, and the three capacitors are tuned to vary the frequency of oscillation. These phase-shift oscillators generally are useful for frequencies under 100 kHz.

A similar oscillator is the *dual-integration oscillator*, which uses two integrators in series to produce the required 360° of phase shift—each integrator producing 180°.

10.24.2 Wien Bridge Oscillator

One of the most commonly used oscillator circuits is the *Wien bridge oscillator*. It is much more easily tunable over a wide range of frequencies than is the phase-shift oscillator of the preceding section, and it produces a low-distortion sinusoidal output. One way of drawing the circuit is shown in Fig. 10.32(a); we have a simple inverting amplifier circuit with feedback taken from the output back to the noninverting input of the op amp. At very high frequencies there is zero positive feedback because the lower capacitance acts as a short circuit, whereas at very low frequencies there is also essentially zero positive feedback because the upper capacitor acts like an infinite impedance. Thus, we immediately expect positive feedback at some finite nonzero frequency that depends on the values of R and C.

Redrawing the circuits as in Fig. 10.32(b) shows us that we have a bridge (the Wien bridge) with the two inputs to the op amp connected where the meter of the analogous *Wheatstone bridge* [Fig. 10.32(c)] would be. The output of the op amp drives the bridge. If the op amp is not saturated, we can apply the OAVR and conclude that the bridge is balanced—the voltage at points A and B must be the same. Thus, we can immediately write the balance condition

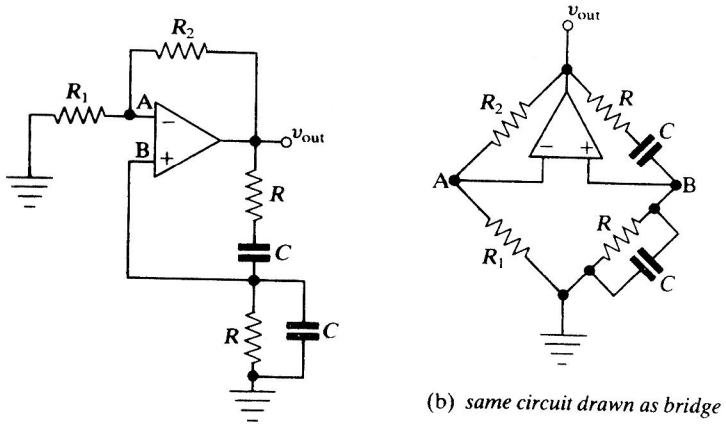
$$\frac{R_2}{R_1} = \frac{Z_4}{Z_3}$$

where Z_4 is the impedance of the series RC arm, $Z_4 = R + 1/j\omega C$, and Z_3 is the impedance of the parallel RC arm, $Z_3 = 1/(1/R + j\omega C)$. Substituting in for Z_4 and Z_3 in the balance equation yields

$$\frac{R_2}{R_1} = 2 + j\left(\omega RC - \frac{1}{\omega RC}\right)$$

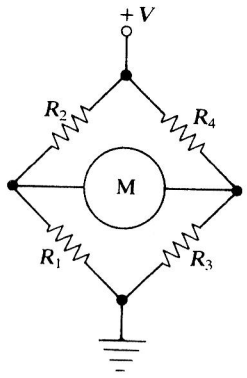
Equating the real and the imaginary parts implies

$$\frac{R_2}{R_1} = 2 \quad \text{and} \quad \omega RC = \frac{1}{\omega RC} \quad \text{or} \quad \omega = \frac{1}{RC} \qquad \textbf{(10.35)}$$



(a) *circuit*

(b) *same circuit drawn as bridge*



(c) *dc Wheatstone bridge for comparison*

FIGURE 10.32 The Wien bridge oscillator.

Thus we see that the bridge is balanced only at the frequency $\omega_0 = 1/RC$ and that the gain of the op amp inverting amplifier must be 2.

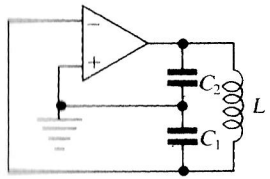
If there is too little gain (R_2/R_1 is too small), the circuit will not oscillate. If there is too much gain, the output will be a distorted sine wave. Thus, the resistance ratio R_2/R_1 is usually made adjustable. The amplitude of the output can be regulated by changing the R_2/R_1 ratio with some long time-constant feedback. If the output amplitude increases, we should make the ratio smaller; if the output decreases, we should make the ratio larger. The principal mechanism that changes the output amplitude is a *thermal* one—if any factor increases the output amplitude, both R_2 and R_1 heat up

due to the larger current flowing through them, whereas if the output amplitude decreases, both R_2 and R_1 cool down. Thus, to stabilize the output amplitude, we want R_2/R_1 to decrease with increasing temperature and to increase with decreasing temperature. This can easily be accomplished by having a negative temperature coefficient for R_2 and/or a positive temperature coefficient for R_1. A thermistor can be used for R_2 because it has a negative temperature coefficient; an incandescent lamp is often used for R_1 because it has a positive temperature coefficient.

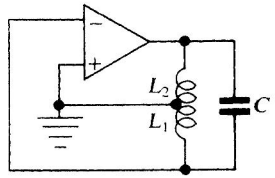
The oscillator frequency can be adjusted by varying R or C. C is usually varied by using air capacitors "ganged" together, which means the same shaft changes both capacitances; R can be changed by a ganged selector switch.

10.24.3 *LC* Oscillators

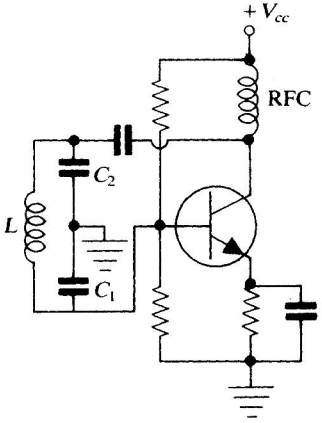
At frequencies above several hundred kHz, most sine-wave oscillators are made with LC resonant circuits. At lower frequencies the inductance would be too large physically to use an LC circuit. Two of the most popular are the Colpitts and the Hartley shown in Fig. 10.33. These circuits can operate



(a) *Colpitts oscillator*



(b) *Hartley oscillator*



(c) *transistor Colpitts oscillator*

FIGURE 10.33 *LC* oscillator circuits.

at frequencies up to many MHz, and with proper component choice they can have a frequency stability of ±0.01% or better. Both the Colpitts and the Hartley circuits feed back a fraction of the op amp output to the inverting input; the 180° phase shift across the LC network plus the 180° phase shift at the output of the op amp produces the positive feedback necessary for oscillation.

The two series capacitors in the Colpitts oscillator have a total capacitance of $C = C_1C_2/(C_1 + C_2)$, so the resonant frequency is

$$\omega_0 = \frac{1}{\sqrt{\frac{LC_1C_2}{C_1 + C_2}}} \tag{10.36}$$

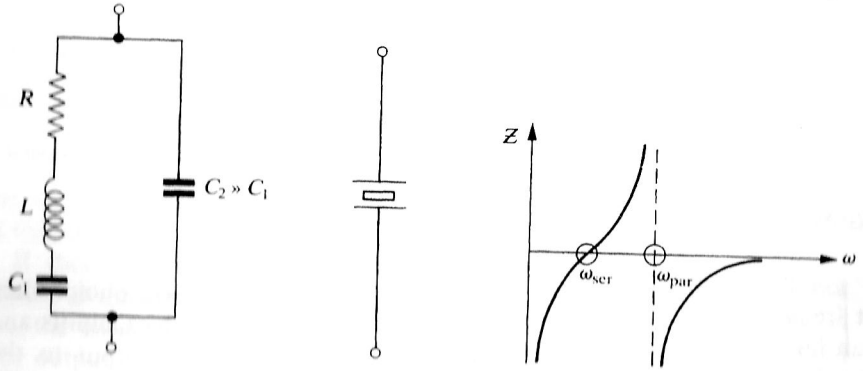
The oscillation frequency may be considerably less in the op amp oscillator circuit than in the bare LC_1C_2 circuit: the smaller C_1 is, the larger the amplitude of oscillation is and the more distortion produced. A similar argument for the Hartley circuit shows that its oscillation frequency is

$$\omega_0 = \frac{1}{\sqrt{(L_1 + L_2)C}} \tag{10.37}$$

Very few op amps can operate at frequencies much over 10 MHz, so at higher frequencies the Colpitts and Hartley circuits are usually used with individual high-frequency transistors that can operate up to 100 MHz or higher. A Colpitts oscillator with a discrete transistor is shown in Fig. 10.33(c).

10.24.4 Crystal Oscillators

Better frequency stability is obtained when the LC resonant circuit is replaced by a quartz piezoelectric crystal. A *piezoelectric crystal* is one in which a mechanical strain produces a voltage difference, and vice versa. The crystal basically acts as a very high-Q LC resonant circuit; its equivalent circuit is shown in Fig. 10.34(a). The capacitance C_2 is between the metal plating applied to the opposite faces of the crystal; the capaci-



(a) *crystal equivalent circuit* (b) *crystal circuit symbol* (c) *crystal impedance vs. frequency*

FIGURE 10.34 Piezoelectric crystal.

tance C_1 is inherent in the crystal. C_2 is invariably much larger than C_1. There are two resonant frequencies: the series resonant frequency of L and C_1, and the resonant frequency of L in parallel with the series combination of C_1 and C_2:

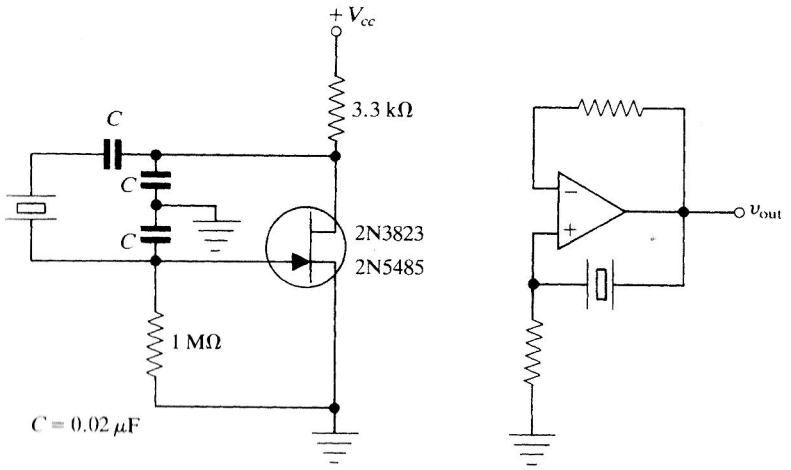
$$\omega_{ser} = \frac{1}{\sqrt{LC_1}} \quad \text{(series)} \tag{10.38}$$

and

$$\omega_{par} = \frac{1}{\sqrt{L\left(\frac{C_1C_2}{C_1 + C_2}\right)}} \quad \text{(parallel)} \tag{10.39}$$

Because $C_2 \gg C_1$, the series and parallel resonant frequencies are very nearly equal, typically within 1%. The reactance of the crystal versus frequency is shown in Fig. 10.34(c). The crystal is inductive for frequencies between the two resonant frequencies (for $\omega_{ser} < \omega < \omega_{par}$), and it is capacitive for frequencies below ω_{ser} and above ω_{par}. The crystal frequency can be tuned by adding a variable capacitor in parallel with the crystal, which effectively changes C_2. Only a slight change in the crystal resonance can be produced by this technique because C_1, not C_2, is the primary determinant of the frequency. The crystal oscillator in a quartz clock or watch oscillates at precisely 32.768 kHz and is divided by 2^{15} to yield a 1-Hz frequency. A piezoelectric crystal can be used in any oscillator circuit, in a Colpitts or a Hartley, for example, to replace the LC tank.

A crystal Colpitts oscillator circuit is shown in Fig. 10.35(a) with an



(a) *Colpitts* (b) *op amp*

FIGURE 10.35 Crystal oscillators.

FET instead of an op amp, and an op amp oscillator circuit is shown in Fig. 10.35(b).

The frequency stability of a typical inexpensive crystal depends on the temperature changes and the power supply voltage changes. It is easy to obtain an overall stability of 0.1 ppm (one part in 10^7) or better with no special precautions. If the temperature is regulated (in a constant-temperature oven) and the power supply voltage is regulated, stabilities better by factors of 10 or 100 are obtainable. Commercial *temperature-compensated crystal oscillators* (TCXO) are available with a frequency stability of 1 to 0.1 ppm over a 50°C range. Over a relatively short time (hours) a frequency drift of only a few parts in 10^{11} is obtainable from a commercial crystal oscillator. For a frequency stability of one part in 10^{12}, we must use an atomic beam apparatus.

PROBLEMS

1. Derive the voltage gain expression (10.14) for a differential amplifier.
2. Derive the voltage gain expression (10.15) for the instrumentation amplifier.
3. Design a one-transistor emitter follower power-booster circuit to amplify the output from an op amp. The output should be able to swing both positive and negative with respect to ground.
4. For the amplifier of Fig. 10.6(c), prove that the voltage gain

$$A = 1 + \frac{R_2}{(1 + j)R_1}$$

when $\omega = \omega_2 = 1/R_2C_2$.

5. For the amplifier of Fig. 10.6(b) prove that the voltage gain

$$A = 1 + \frac{j}{1 + j}\left(\frac{R_2}{R_1}\right)$$

when $\omega = \omega_1 = 1/R_1C_1$.

6. Design an op amp amplifier (noninverting) that will amplify signals from approximately 50 Hz to 10 kHz with a gain of 20. Frequencies below 50 Hz and above 10 kHz should be attenuated.
7. Design a summing amplifier circuit to sum from inputs v_A, v_B, v_C, v_D and to produce an output of $v_{out} = v_A + 2v_B + 4v_C + 8v_D$.
8. Design a current-to-voltage converter to convert a 1-μA input to a 2-V output. The 1-μA current input has (signal) Fourier components up to 100 Hz, and higher frequency noise is present.
9. Design a voltage-to-current converter to convert a 1-mV input voltage to a 1-mA current through a 1-kΩ load resistor.
10. Design a current-to-current converter (or current multiplier) to produce a 10-mA output for a 100-μA input.

11. For the logarithmic amplifier show that if an input v_1 produces an output V_1 and v_2 produces V_2,

$$V_2 - V_1 = \left(\frac{kT}{e}\right)\ln\left(\frac{v_2}{v_1}\right)$$

12. If in the logarithmic amplifier, the input $v_1 = 10$ mV for an output $V_1 = -0.04$ V, calculate R if $I_0 = 10^{-10}$ A. Calculate the output for an input $v_2 = 100$ mV.
13. Design an ideal diode op amp circuit to produce a *negative* half-waveform from a sinusoidal input.
14. Design an ideal diode (op amp) clamp circuit to produce an output voltage clamped to +5 V; that is, $v_{out} \geqq 5$ V. Sketch the input and output waveforms for an arbitrary input.
15. Design an ideal (op amp) half-wave rectifier to produce a half-wave output that is twice the amplitude of the input. Repeat for an ideal (op amp) full-wave rectifier.
16. Design a (op amp) peak detector circuit. Is a bipolar or an FET op amp better? Calculate the approximate droop rate in volts per second if $C = 0.001$ μF and the op amp input impedance is 10^{10} Ω.
17. Design a sample-and-hold circuit. Calculate the droop rate if $I_B = 100$ pA and $C = 0.01$ μF. What are the two conflicting requirements for C? If $\Delta\tau$ is the time between successive samples, explain why we desire

$$R_{MOSFET}C \ll \Delta\tau$$

18. Design an op amp differentiator whose output is

$$v_{out} = -(10^{-6})\frac{dV_{in}}{dt}$$

If an input step function rises from 0 to 1 V in 2 μs and then is constant at 1 V, sketch the output.

19. Design an op amp integrator whose output is

$$v_{out} = -10^4 \int v_{in}\, dt$$

20. The comparator is bipolar. (a) Sketch the output waveform if $V_{bb} = +5$ V. (b) Repeat for $V_{bb} = -5$ V. (c) How would you change the circuit to produce output voltages of +5 V and −0.6 V?